83306800

CONTROL DATA CORPORATION

CONTROL DATA®
DISK STORAGE UNIT
BR3C2

GENERAL DESCRIPTION
OPERATION
THEORY OF OPERATION

HARDWARE REFERENCE MANUAL

LIST OF EFFECTIVE PAGES

Sheet 1 of 1

New features, as well as changes, deletions, and additions to information in this manual are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

PAGE	REV
Cover	-
Blank	-
Title Page	-
ii	D
ii.i/ ii.ii	D
Blank	-
iii/iv	A
Blank	-
v	B
vi	C
Div.Sheet	-
Blank	-
1-1	C
1-2	B
1-3	C
1-4	C
1-5	C
1-6	B
Div.Sheet	-
Blank	-
2-1	A
2-2	A
2-3	A
2-4	A

PAGE	REV
2-5	A
2-6	A
2-7	A
2-8	A
2-9	A
2-10	A
2-11	A
2-12	A
2-13	A
2-14	A
Div.Sheet	-
Blank	-
3-1	B
3-2	A
3-3	B
3-4	B
3-5	A
3-6	B
3-7	B
3-8	B
3-9	B
3-10	B
3-11	A
3-12	A

PAGE	REV
3-13	D
3-14	D
3-15	B
3-16	A
3-17	B
3-18	A
3-19	B
3-20	B
3-21	B
3-22	C
3-23	A
3-24	C
3-25	A
3-26	A
3-27	C
3-28	C
3-29	A
3-30	A
3-31	A
3-32	A
3-33	A
3-34	A
3-35	A
3-36	A

PAGE	REV
3-37	A
3-38	A
3-39	A
3-40	A
3-41	A
3-42	A
3-43	A
3-44	B
3-45	B
3-46	B
3-47	A
3-48	A
3-49	A
3-50	A
3-51	A
3-52	A
3-53	A
3-54	A
3-55	A
3-56	A
3-57	A
3-58	A
3-59	A
3-60	A

PAGE	REV
3-61	A
3-62	A
3-63	A
3-64	A
3-65	A
3-66	A
3-67	A
3-68	A
3-69	A
3-70	A
3-71	A
3-72	A
3-73	A
3-74	A
3-75	A
3-76	A
3-77	A
Blank	-
Cmt.Sht.	-
Envelope	-
Blank	-
Cover	-

REVISION RECORD

REVISION	DESCRIPTION
A	Manual Released
(4-15-74)	
B	Manual updated with Engineering Change Orders PE35350A, PE35586A, PE35634C. Technical
(5-22-75)	and editorial changes. Affects pages: v, 1-1 thru 1-5, 1-6 (added), 3-1, 3-3, 3-4, 3-6 thru 3-10,
	3-13 thru 3-15, 3-17, 3-19 thru 3-21, 3-44 thru 3-46.
C	Manual updated with Engineering Change Order PE35829B. Technical and editorial changes.
(9-12-75)	Affects pages: Cover, vi, 1-1, 1-3, 1-4, 1-5, 3-22, 3-24, 3-27, 3-28.
D	Manual updated with Engineering Change Order 35884 and editorial changes.
(12-5-75)	

Publication No.
83306800

Address comments concerning this manual to:
Control Data Corporation
Technical Publications Department
7801 Computer Avenue South
Minneapolis, MN 55435

or use Comment Sheet in the back of this manual.

Printed in the United States of America

PREFACE

This manual has been prepared for customer engineers and other technical personnel directly involved with maintaining the disk storage unit (drive).

Reference information is provided by three sections in this manual. Section numbers and a brief description of their contents are listed below:

Section 1 - General Description. Describes equipment functions, specifications, and equipment number identification.

Section 2 - Operation. Describes and illustrates the location and use of all controls and indicators, power on sequencing, and disk pack installation and removal.

Section 3 - Theory of Operation. Describes basic logic and mechanical functions.

Manuals applicable to the BR3C2A Disk Storage Unit. are as follows:

Publication No.	Title
83306700	Maintenance
83306800	Reference
83306900	Parts Data
70629100	Logic Cards

CONTENTS

FIGURES

TABLES

SECTION 1

GENERAL DESCRIPTION

INTRODUCTION

The CONTROL DATA® BR3C2 Disk Storage Unit is high speed, random access, disk storage device. Data is recorded on removable disk packs.

Equipment specifications are listed in Table 1-1.

TABLE 1-1. DRIVE SPECIFICATIONS

Characteristic	Conditions	Specifications
PHYSICAL SPECIFICATIONS		
Size	Height	39.5 in. (100 cm)
	Width	22 in. (56 cm)
	Depth	44.5 in. (176 cm)
Weight		660 lbs (300 kg)
Temperature	Operating	60°F (15.5°C) to 90°F (32°C)
	Gradient	12°F (6.6°C) per hour
	Non-Operating	-30°F (-34°C) to +150°F (66°C)
Relative Humidity (no condensation)	Operating	20% to 80%
	Non-Operating	5% to 95%
Altitude	Operating	-1000 ft (-305 m) to +10,000 ft (3.05 km) mean sea level
	Non-Operating	-1000 ft to +35,000 ft (10.7 km)
POWER SPECIFICATIONS (Typical Values)		
Refer to Pub. No. 83306700 for additional power information. Definitions: Standby State: dc power on, spindle motor off. Accessing State: positioner continually random seeking.		
AC Power Input	BR3C2A	208v (±10%), 60 (±0.6) Hz, 3Ø
	BR3C2B	380v (±10%), 50 (±0.5) Hz, 3Ø
	Phasing (60 Hz)	Two phases supplied from a three-phase delta source are used per 60 Hz drive. Three-phase power is available at A1TB1 by power cable. During installation, two phases are connected internally. Phases are normally rotated from drive-to-drive externally so that each group of three drives present a balanced three-phase load. Motors are single-phase connected phase-to-phase.
	Phasing (50 Hz)	One phase is used per 50 Hz drive. Three-phase power available at A1TB1 by power cable. Power is connected phase-to-neutral neutral with phases rotated internally from drive-to-drive to present a balanced three-phase load.
Current		
208v at 60 Hz	Standby	2 amp/phase
	Starting	38 amp/phase for 9 sec.
	Accessing	8 amp/phase

TABLE 1-1. DRIVE SPECIFICATIONS (Cont'd)

Characteristics	Conditions	Specifications
Current		
220v at 50 Hz	Standby	2.5 amp/phase
	Starting	39 amp/phase for 8 sec.
	Accessing	9.5 amp/phase
Power (True)		
208v at 60 Hz	Standby	0.4 kilowatt
	Accessing	1.2 kilowatt
220v at 50 Hz	Standby	0.5 kilowatt
	Accessing	1.3 kilowatt
Power Factor		
208v at 60 Hz	Standby	0.9
	Accessing	0.7
220v at 50 Hz	Standby	0.9
	Accessing	0.6
Heat Dissipation		
208v at 60 Hz	Standby	1400 BTU/hr (353 kg-cal/hr)
	Accessing	4200 BTU/hr (1060 kg-cal/hr)
220v at 50 Hz	Standby	1750 BTU/hr (440 kg-cal/hr)
	Accessing	4500 BTU/hr (1135 kg-cal/hr)
DATA RECORDING SPECIFICATIONS		
Disk Pack	Packs/Drive	1
	Recording Surfaces/ Disk Pack	19
	Usable Tracks/ Recording Surface	411 (404 plus 7 spares)
	Tracks/Cylinder	19
	Tracks/Inch	192
	Track Spacing	0.0052 inch (nominal)
	Rotational Speed	3600 (±2%) rpm (16.7 ms/rev)
	Recommended Pack	CDC 881
Seek Timing	Access Mechanism	Voice Coil driven by servo loop
	403 Tracks	55 milliseconds (maximum)
	1 Track	10 milliseconds (maximum)
	Average	30 milliseconds
Latency Time	Average	8.33 milliseconds (@ 3600 rpm)
	Maximum	17 milliseconds (@ 3528 rpm)
Recording	Mode	Modified Frequency Modulation (MFM)
	Bit Density	4040 bpi (inner track nominal)
	Rate	6.45 MHz (nominal)

TABLE 1-1. DRIVE SPECIFICATIONS (CONT'D)

Characteristics	Conditions	Specifications
Heads	Quantity	19 recording 1 servo (positioning)
	R/W Gap	0.030 in (nominal)
	Read/Write Width	0.004 in (nominal)
Data Capacity	Bits/Byte	8
	Bytes/Track	13,440 ← NUMBER OF DI BITS AROUND PACK
	Bytes/Cylinder	255,360 = 19 X 13440
	Bytes/Spindle	103,165,440 → 404 X 25360
	Tracks/Cylinder	19
	Cylinders/Unit	404 (+7 spares)
Controller/Drive	Quantity	2 per drive
Interface Cables	Maximum Length	75 ft (22.8 meters)
	Connectors	2 per drive
	Pin Assignments	Refer to Publication No. 83306700
	Signal Functions	Refer to Section 3 of this manual

ASSEMBLY LOCATIONS

Figure 1-1 illustrates the major drive assemblies. Detailed information on the construction and function of these assemblies is provided in Section 3 of this manual.

TOP COVER ASSEMBLY

The top cover assembly protects the drive assemblies during customer operations. The entire assembly may be exposed for maintenance by raising the top cover (from the rear) and the pack cover.

The pack cover is released by a latch at the front of the unit. An electrical switch senses that the cover is opened and disables spindle power.

DECK ASSEMBLY

The deck assembly has the following major sub-assemblies:

- A spindle assembly to mount the disk pack. Its associated drive motor runs continuously whenever a pack is installed, the pack cover is closed, the START switch is on, and sequence power (either from the controller or with the LOCAL/REMOTE switch in the logic door in the LOCAL position) are available.
- An actuator assembly that mounts the read/write heads for processing data. The actuator contains a voice coil positioner controlled by a closed-loop, continuous-feedback servo system.

16.66 ms / 806 KHZ = 13,433

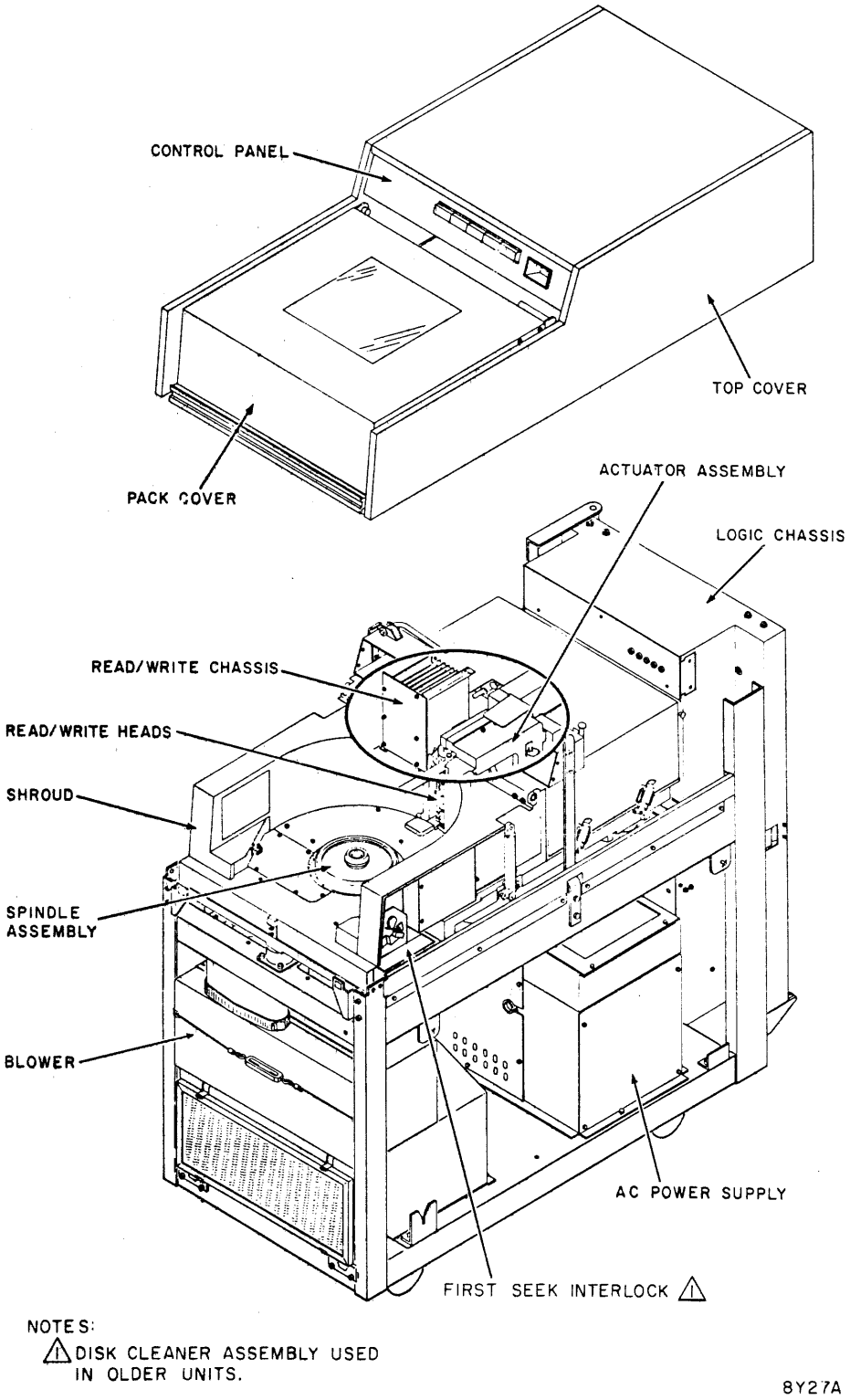


Figure 1-1. Assembly Locations

- A shroud to surround the disk pack. The shroud: protects the pack, aids in directing air from the blower to the pack, and prevents the operator from damaging the read/write heads with the pack.
- A read/write chassis to mount logic cards that contain logic directly affecting head selection and operation.
- A disk cleaner assembly to clean the disks during power up sequences is used in S/C 09 without PE35634C and Below. A timing motor and switch assembly to delay head loading for approximately 15 seconds on power up sequences used in S/C 09 with PE35634C and Above.

AC POWER SUPPLY

The ac power supply provides ac power required by the drive. The ac voltages generated are distributed to the dc power supply located in the logic chassis assembly.

The line filter filters the ac power input to the power supply.

LOGIC CHASSIS

The logic chassis serves as the mounting point for the main complement of the logic cards and dc power supply. The chassis is hinge-mounted for easy access to the cards (which plug in at the inner side of the chassis) or to the backpanel terminals (at the outer side). The backpanel terminals provide ready access to all signals entering and leaving each card. In addition, the cards have test points for monitoring critical signals within the cards.

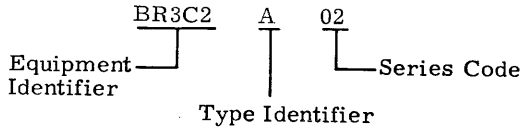
The logic chassis also contains a test point panel that provides a location for status monitoring of the dc voltages generated by the dc power panel.

Located in the lower half of the logic chassis is the dc power panel. The dc power panel provides dc power required by the drive. It also contains relays and solid state logic used for power sequencing.

EQUIPMENT IDENTIFICATION

An equipment number is assigned to each drive to identify its configuration. This provides a systematic method of identifying, accounting, and controlling changes that affect drive logic and mechanical components.

The equipment configuration is identified by a nameplate attached to the frame at the back of the drive. The nameplate is visible with the logic chassis open. The Equipment Identification Number will be similar to the following:



The Equipment Identifier indicates the basic function of the unit. This number will be BR3C2 on all units for which this series of manuals have been prepared.

The Type Identifier indicates a non-interchangeable difference in equipments that affects the interface. The term "Mod" is sometimes used interchangeably with "Type Identifier". The following identifiers have been assigned:

Engineering Number	Channel Configuration	Volts/ Frequency
BR3C2A	Single	208/60 Hz
BR3C2B	Single	308/50 Hz

The Series Code changes with each non-interchangeable change within the equipment. Drives with different series codes are fully interchangeable at the system level; however, not all of their electrical or mechanical components may be interchangeable. Series codes are changed by Engineering Change Order (ECO) only at the factory.

Other changes are accomplished by Field Change Order (FCO). These changes may be installed either at the factory or by field personnel. FCO changes are indicated by an entry on the FCO Log that

accompanies each machine. It is important that this log be kept current by the person installing each FCO.

Unless otherwise specified, all theory, procedures, and diagrams in these manuals apply to all units. Exceptions are noted where applicable.

Manuals accompanying unit shipments from the manufacturer match the configuration of those units. Subsequent manual changes are controlled by the Revision Record sheet behind the title page of every manual. This sheet identifies the Series Code and FCO effectivity of manual changes. If maintenance will be performed using a manual other than the manual supplied with each drive, verify that the manual and drive configurations match.

SECTION 2

OPERATION

CONTROLS AND INDICATORS

The drive contains several panels and indicators. Figure 2-1 locates the panels and indicators on a cabinet. Table 2-1 and 2-2 describe the various panel controls and indicators.

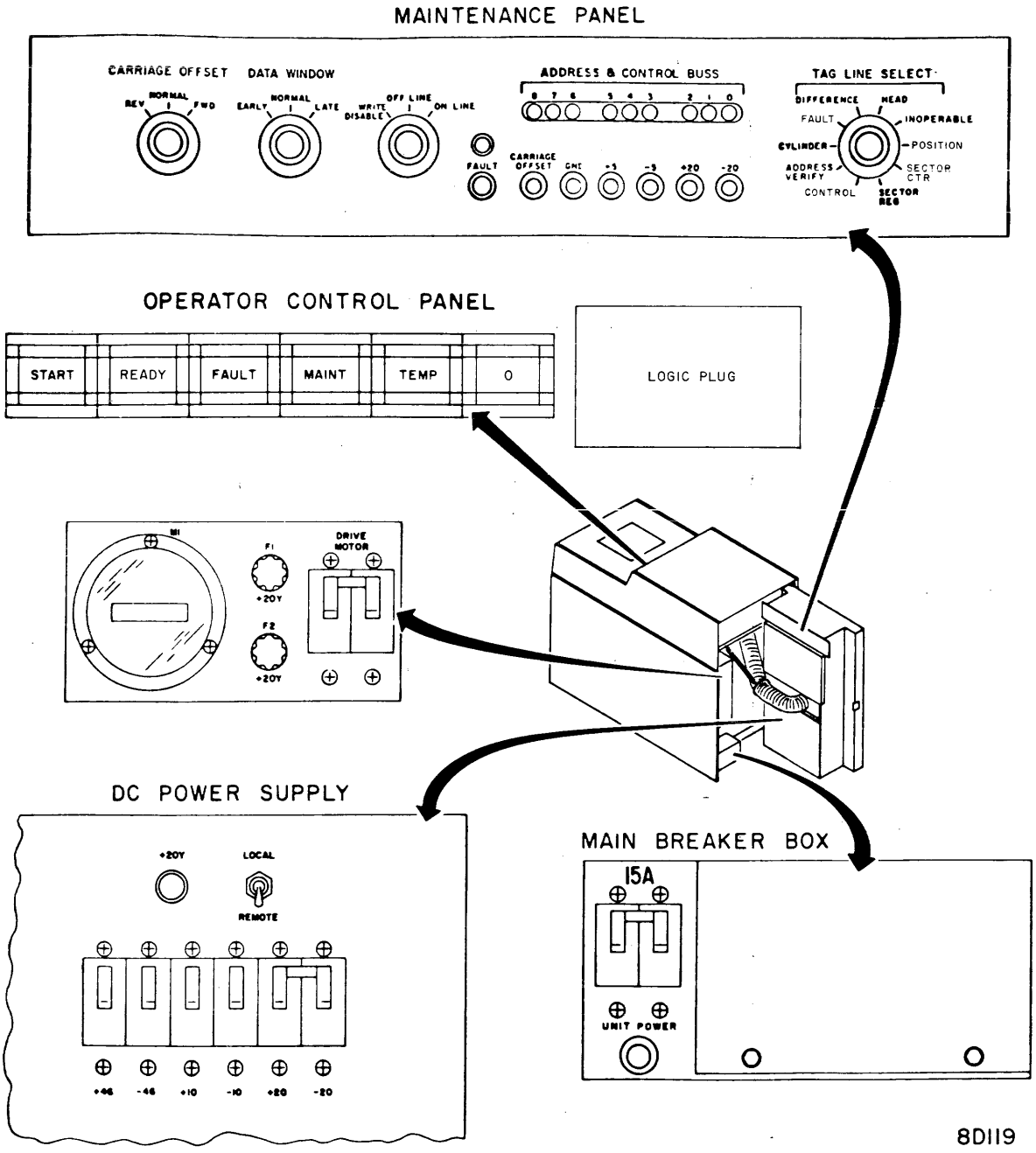


Figure 2-1. Controls and Indicators

TABLE 2-1. CONTROLS AND INDICATORS

Control or Indicator	Function
	Operator Panel
START switch/indicator	Switch energizes (when pressed to light) spindle drive motor and begins the First Seek sequence provided the following conditions are met: 1. Disk pack is in place and canister removed. 2. Pack cover is closed. 3. Circuit breakers are on. 4. Sequence power available either from control unit (if power supply panel LOCAL/REMOTE switch is set to REMOTE) or from power supply (if power supply LOCAL/REMOTE switch is set to LOCAL). Lights when switch is on and conditions 2 and 3 are met. This allows operator to know which units will sequence on when control unit sequence power becomes available. Switch causes a power off sequence when pressed while the indicator is lighted.
READY indicator	Indicator lights when read/write heads are loaded, unit is selected and reserved, and a Power-up first seek is completed.
MAINTENANCE indicator	Lights when related drive has experienced one of the following conditions: 1. LOCAL/REMOTE switch on DC Power Supply Panel set to LOCAL. 2. ON LINE/OFF LINE/WRITE DISABLE switch on Logic Chassis Maintenance panel set to OFF LINE or WRITE DISABLE.
FAULT switch/indicator	Lights when one or more of the following unwanted conditions occur: (pressing switch clears Fault FF only) 1. No data transitions for 900 nsec while Write Enable is up. 2. Read or Write gate is up while unit is not on cylinder. 3. Voltage fault- Low voltage (±5v, ±20v, or -16v). If -16v is low, heads retract. 4. No servo tracks - loss of servo tracks for 200 msec. 5. Read and Write are selected at the same time. 6. More than one head is selected.

TABLE 2-1. CONTROLS AND INDICATORS (Cont'd)

Control or Indicator	Function
LOGIC PLUG/switch	The plug is not an accessory item and is interchangeable. When inserted, it activates a switch which determines Unit Available status.
TEMP (Temperature) indicator	Indicates above normal temperature in logic chassis.
UNIT NUMBER indicator	Lights when the drive is selected. Significance of this number (0 through 7) indicates unit designation within the system.
Logic Chassis Maintenance Panel	
CARRIAGE OFFSET switch	NOTE The CARRIAGE OFFSET switch is designed for use during a maintenance situation. Function of the switch is enabled only when the ON LINE/OFF LINE/ WRITE DISABLE switch is in the OFF LINE or WRITE DISABLE positions. NORMAL position allows servo logic to position carriage to the nominal center of the disk pack servo track. REV position injects a fixed bias so that carriage is positioned 400 microinches off nominal center of servo track in the direction away from the spindle. FWD position injects a fixed bias so that carriage is positioned 400 microinches off nominal center of servo track in the direction toward the spindle.
DATA WINDOW switch	NORMAL position allows data strobe to occur in the nominal center of the allowable margin of the data window (time period in which a recovered data "1" must appear in order to be recognized as a "1"). EARLY position causes data strobe to be moved to the early margin position of the data window. LATE position causes data strobe to be moved to the late margin position of the data window. (Data strobe occurs about 8 nsec later than normal.)
ON LINE/OFF LINE/ WRITE DISABLE switch	ON LINE position places drive under control of the control unit. OFF LINE position inhibits selected signals to and from control unit and enables the CARRIAGE OFFSET and DATA WINDOW switches. WRITE DISABLE position causes same occurrences as for OFF LINE position and additionally disables the Write circuits.

TABLE 2-1. CONTROLS AND INDICATORS (Cont'd)

Control or Indicator	Function
FAULT switch/indicator	Lights in response to one or more of the same conditions as listed for the operator panel FAULT switch/indicator. Pressing the logic chassis maintenance panel FAULT switch or switching ON LINE/OFF LINE/WRITE DISABLE switch from OFF LINE to ON LINE clears the Fault FF and all bits of the Fault register.
CARRIAGE OFFSET test jack	NOTE The CARRIAGE OFFSET test jack is used in conjunction with the CARRIAGE OFFSET switch. Affords a point at which an external resistance to ground can be applied to cause various carriage offsets to either side (forward or reverse) of the nominal center of the servo track. Direction of the offset is controlled by the CARRIAGE OFFSET switch. Resistance (to gnd) — Offset (in microinches) 470 ohms — 750 1 K — 700 2.2 K — 650 4.7 K — 600 8.2 K — 550 12 K — 500 27 K — 450 Open — 400
GND, +5, -5, +20, -20, and GND test jacks	Provide points at which dc voltages in logic chassis can be measured.
ADDRESS & CONTROL BUSS bit indicators (9)	Display information as selected by TAG LINE SELECT switch. Buss bit indicator lights if selected signal is true. Refer to TAG LINE SELECT switch for information displayed at each switch position.
TAG LINE SELECT switch	The TAG LINE SELECT switch is designed for use during a maintenance situation. Function of the switch is enabled only when the drive is in an off line condition. The ten position rotary switch allows selection and display of current machine status and register contents. (Refer to Table 3-1 for detailed signal description.)
AC Power Supply	
Elapsed time meter	Indicates cumulative hours that logic dc power is on.
DRIVE MOTOR circuit	Controls application of ac voltage to spindle drive motor.
+20Y Fuses	Protects 20 volt power supply transformer used to derive +20Y sequence and lamp voltages.

TABLE 2-1. CONTROLS AND INDICATORS (Cont'd)

Control or Indicator	Function
DC Power Supply	
+20Y indicator	Lights to indicate presence of +20Y voltage used by lamps and power up sequence circuit.
LOCAL/REMOTE switch	Allows power up sequence to be controlled by either the control unit (when set to REMOTE) or by +20Y-vdc from power supply (when set to LOCAL).
±46, ±20, and ±10 volt circuit breakers	Control application of related dc voltages throughout drive.
Main Breaker Box	
UNIT POWER circuit breaker	Controls application of main ac power.

TABLE 2-2. ADDRESS AND CONTROL BUS INDICATORS

TAG LINE SELECT Switch Setting *	Indicator Bit Meanings								
	8	7	6	5	4	3	2	1	0
ADDRESS VERIFY**	256	128	64	32	16	8	4	2	1
CYLINDER	256	128	64	32	16	8	4	2	1
FAULT	Address Error Fault**	Not Used	Not Used	Seek Error	-Volt	+Volt	Current	W●R	(W+R)● Not On Cylinder
CONTROL	Not Used	Not Used	End of Cyl.	Not Used	Index	On Cyl.	Seek Error	Pack Unsafe	Not Used

NOTES:

*Positions of the Tag Line Select rotary switch other than those listed in this table are not wired and therefore ineffectual.

**Functional only when drive is being used with Off Line Tester. FAULT indicator does not light, but switch must be pressed to clear this bit in drive Fault register.

OPERATING INSTRUCTIONS

POWER APPLICATION

The following procedure prepares the drive to go on line.

1. Install a disk pack (refer to Disk Pack Installation).
2. Open logic chassis door and position logic chassis maintenance panel switches as follows:
   - CARRIAGE OFFSET switch to NORMAL.
   - DATA WINDOW switch to NORMAL.
   - ON LINE/OFF LINE/WRITE DISABLE switch to ON LINE.
3. Set main breaker box UNIT POWER circuit to ON. Blower motor will begin to operate.
4. Open cabinet logic Chassis door and position DC power supply switches as follows:
   a. LOCAL/REMOTE switch to REMOTE. Power up sequence is then under system control. If maintenance is to be performed, set switch to LOCAL.

   NOTE

   If LOCAL is selected, all drives with higher UNIT NUMBER indicator designations may also be powered on. For example, if unit 2 is set to LOCAL, any of the units 3 through 7 with packs installed and START switch on will power on.

   b. Set all circuit breakers to ON.
5. The power supply +20Y indicator lights.
6. Close cabinet logic chassis door.
7. Press operator panel START switch/indicator. The switch/indicator lights.
8. When control unit sequence power becomes available, or if in LOCAL mode, the First Seek operation begins.
9. The First Seek operation is complete when the heads are positioned at track 00. READY indicator lights when the First Seek operation has been completed. The unit is now ready to receive a command.

DISK PACK HANDLING

To ensure maximum disk pack life and reliability, observe the following precautions:

1. Store disk packs in a machine-room atmosphere (60°F to 90°F, 10% to 80% relative humidity).
2. If a disk pack must be stored in a different environment, allow two hours for adjustment to the computer environment before use.
3. Never store a disk pack in sunlight, in a dirty environment, or on top of another disk pack.
4. Store the disk packs flat, not on edge.
5. Always be sure that both the top and bottom plastic covers are on a disk pack whenever it is not actually installed in a drive.
6. When marking packs, use a pen or felt-tip marker that does not produce a loose residue. Never use a lead pencil. Write on the label before it is applied to the disk pack.

DISK PACK INSTALLATION

Make certain that the disk pack to be installed has been properly maintained.

1. Raise drive pack cover.
2. Lift the disk pack by the plastic canister handle.
3. Disengage the bottom dust cover from the disk pack using the knob in the center of the cover. Set the cover aside to an uncontaminated storage area.

CAUTION

Avoid abusive contact between the disk pack and the spindle. During maintenance procedures the read/write heads are sometimes manually positioned. Make certain the heads are fully retracted.

4. Place the disk pack onto the spindle.

NOTE

A spindle lock mechanism (ratchet brake) is actuated when the disk pack canister cover is on the spindle. A "click" may be heard as the lock mechanism engages. The mechanism holds the spindle stationary while loading or unloading a disk pack.

5. Twist the canister handle clockwise until pack is locked in place.
6. Lift the canister clear of the disk pack and set it aside to an uncontaminated storage area.
7. Close the front cover immediately to prevent the entry of dust and the contamination of the disk surfaces.

DISK PACK REMOVAL

1. Press (to extinguish) the operator panel START switch.
2. Check that disk pack rotation has stopped completely.
3. Raise the front cover.

CAUTION

During maintenance procedures the read/write heads are sometimes manually positioned. Make certain that the heads are fully retracted.

4. Place the plastic canister over the mounted disk pack so that the post protruding from the center of the disk pack is received into the canister handle.
5. Twist the canister handle counterclockwise until the disk pack is free of the spindle.

CAUTION

Avoid abusive contact between the disk pack and the spindle assembly.

6. Lift the canister and the disk pack clear of the spindle.
7. Close the front cover.
8. Place the bottom dust cover in position on the disk pack and tighten it.
9. Store the disk pack in a clean cabinet or on a clean shelf.

HEAD ALIGNMENT CARD

Four LED indicators are provided as monitors to ensure accurate alignment data is taken. Their functions are:

Power - When lighted indicates power is applied to card (card is fully inserted in card slot).

Input - When lighted indicates amplitude of alignment signal is below minimum threshold required to allow alignment card to operate.

Bad Track - When lighted indicates short duration loss of alignment signal. Indicator lights when polarity switch (S1) is operated. A one-shot maintains light for four seconds.

Mode - When lighted indicates switches S2 (servo-R/W select) or S3 (meter sensitivity) are not in correct position to measure data head alignment error.

NOTE

Measurement of data head alignment error can be taken only when the power indicator is on and the other indicators are off.

Three toggle switches are provided on the card edge which perform the following functions:

S1 - Switch changes the polarity of the alignment signal and is used in taking measurements of both servo and data heads as follows:

a) note null meter reading in P (normal position)

b) note null meter reading in N (reverse position)

then P-N=alignment position, i.e., P=+30 mv, N=-40 mv (+30)-(-40)= +70 mv alignment error.

S2 - Switch selects the servo head (S) as an input to the card on the data head(R/W). When switch is in S position, mode indicator will light.

S3 - Switch changes the sensitivity of the meter circuit (TPX and TYP). In X1 position, meter readings are multiplied by 1, in X.1 multiply meter readings by 10. With switch in X1 position, mode indicator lights.

Test points TP-X and TP-Z are connected to the null meter. TP-Y is connected to an oscilloscope to observe the dibit pattern.

OFF LINE TESTER

The tester front panel is illustrated in Figure 2-2. Switch functions are defined in Table 2-3.

The Off Line Tester available for the BR3C2 is P/N 86073403.

All Index-to-Index references are from trailing edge of delayed Index to leading edge of next Index. Delayed Index is 600 μsec after leading edge of Index.

PREPARATION FOR USE

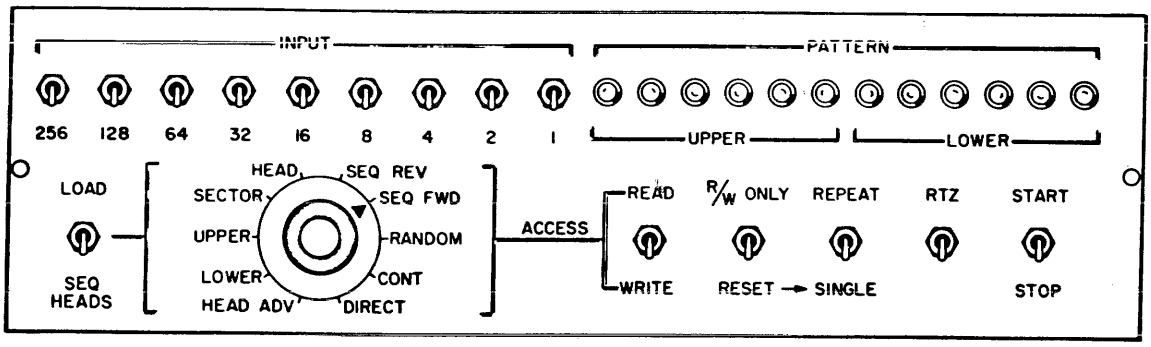
1. Verify that the CPU operating system permits the drive to be removed from computer control.
2. Open cabinet rear door.
3. Set ON LINE/OFF LINE/WRITE DISABLE switch to OFF LINE. Tester will not work in ON LINE mode. If operated in WRITE DISABLE mode, accessing and reading are normal, but data cannot be written.
4. Open tester bottom panel and remove cable assembly. If tester has not been used, verify that 13.60 MHz crystal is installed. The 12.88 MHz crystal should be in the dummy jack. Replace cover.
5. Connect cable assembly between connectors on rear of tester and C26 on logic rack. Tester receives power from drive.

OPERATING PROCEDURES

The TAG LINE SELECT switch on the logic rack maintenance panel is a valuable accessory in using the tester. A thorough knowledge of this switch and its functions will assist greatly in isolating malfunctions. Functions of each switch position are specified in Table 2-2.

When set to ADDRESS VERIFY, the ADDRESS & CONTROL BUSS indicators display the cylinder address read from the disk. This function is enabled only during tester read operations. If any error occurs, all accessing stops and the last address read will be displayed. Proceed as follows:

1. Set TAG LINE SELECT switch to FAULT to verify the type of error. Bit 8 displayed indicates that the tester detected an address error. (On the other hand, bit 5 indicates a seek error.)
2. Set switch to CYLINDER to determine the address that the drive should be at.



NOTES: 1. DATA SYNC JACK IS ON REAR PANEL OF TESTER.
2. SEQ HEADS FUNCTION AND DATA SYNC JACK NOT APPLICABLE TO TESTER, P/N 72841000.

7J122

Figure 2-2. Off Line Tester

TABLE 2-3. OFF LINE TESTER SWITCH FUNCTIONS

Switch/Indicator	Mode Select Switch Position	Function
Bits Used		
INPUT All	DIRECT	Loads destination cylinder of seek.
All	CONT	
All	SEQ FWD	Loads length of each forward or reverse incremental seek.
All	SEQ REV	
1-16	HEAD	Loads head to be selected for read/write operations.
1-32	UPPER	Loads upper six bits of data pattern to be written.
1-32	LOWER	Loads lower six bits of data pattern to be written.
PATTERN lamps	--	Indicates 12-bit data pattern that has been loaded into tester for write operations.
Mode Select	--	Controls tester mode of operation.
	HEAD ADV	Drive head register is incremented each time LOAD switch is actuated. Make sure all INPUT switches are in their down position when using this function.

TABLE 2-3. OFF LINE TESTER SWITCH FUNCTIONS (Cont'd)

Switch/Indicator	Mode Select Switch Position	Function
Mode Select (Cont'd)	LOWER	Loads write data pattern selected by INPUT switches 32 through 1 when LOAD switch is actuated. Pattern is displayed by LOWER PATTERN indicators.
	UPPER	Loads data pattern selected by INPUT switches 32 through 1 when LOAD switch is actuated. Pattern is displayed by UPPER PATTERN indicators.
	SECTOR	Not used.
	HEAD	Selects head to be used for read/write operations (determined by INPUT switches 16 through 1) when LOAD switch is actuated. NOTE The following switch positions, except DIRECT, are under further control of REPEAT/SINGLE switch.
	SEQ REV	Drive seeks in reverse until it reaches cylinder 000; operation then stops. Decrement length selected by INPUT switches.
	SEQ FWD	Drive seeks forward until it reaches cylinder 410 (or address is generated that would exceed 410), then performs direct seek to cylinder 000. Sequence repeats. Increment length selected by INPUT switches.
	RANDOM	Drive continuously seeks forward or reverse to random cylinder. INPUT switches have no effect.
	CONT	Drive continuously seeks from starting by INPUT switches.
LOAD/SEQ HEADS LOAD	UPPER LOWER	Data selected by INPUT switches is loaded into tester.
	HEAD	Data selected by INPUT switches is loaded into drive.
Neutral	--	No data loaded.
SEQ HEADS	SEQ FWD	Head register is automatically incremented by one while access is returning to cylinder 000.

TABLE 2-3. OFF LINE TESTER SWITCH FUNCTIONS (Cont'd)

Switch/Indicator	Mode Select Switch Position	Function
READ/WRITE	Any access position	Refer to REPEAT/SINGLE switch for further information on R/W ONLY.
READ	--	Drive reads selected track with selected head after each seek. Cylinder address read from disk is displayed on logic chassis maintenance panel if its TAG LINE SELECT switch is in ADDRESS VERIFY position. If error occurs on compare between address read from disk and current cylinder address, accessing stops. This may be verified by setting TAG LINE SELECT to ERROR: if bit 2^1 (Device Failure) is lit, Address Error Fault has been detected by tester.
ACCESS (Neutral)	--	Reading and writing inhibited. Only seeks are enabled.
WRITE	--	After each seek, drive writes following pattern from Index-to-Index: 1. Gap of 150 μsec of zeros. 2. Sync bit. 3. Cylinder address. 4. Bit pattern (repeated to end of track) loaded into PATTERN display.
R/W ONLY/RESET		
R/W ONLY	Any	Seeks are inhibited. Refer to REPEAT/SINGLE switch for further information.
Neutral	Any	Seeks enabled. Refer to READ/WRITE.
RESET	CONT	Resets starting address of single-access continuous seeks (SINGLE and CONT).
REPEAT/SINGLE		
SINGLE	Any access	One access will be taken each time START is actuated. If writing, one seek/write operation (Index-to-Index) is performed per START switch actuation. If reading, one seek/read operation (selected track is read) is performed per START switch actuation. In R/W ONLY mode (seeks inhibited), has the following effects:

TABLE 2-3. OFF LINE TESTER SWITCH FUNCTIONS (Cont'd)

Switch/Indicator	Mode Select Switch Position	Function
SINGLE (Cont'd)		1. While writing, one track is written (Index-to-Index) per START switch actuation. 2. While reading, selected track is read once per START switch actuation. Before repeating this operation, selected sector must be reloaded.
REPEAT	Any access	Accessing continues until STOP switch is actuated (except, DIRECT has only one access). If reading or writing, one operation is performed per seek. Writing is Index-to-Index; reading is selected track. In R/W ONLY mode (seeks inhibited), has the following effects: 1. While writing, track is continuously rewritten. 2. While reading, every track is continuously read.
RTZ	Any	Drive performs a return to zero seek.
START/STOP START	Any access	Initiates selected operation. If in SINGLE mode, switch must be actuated for each execution.
STOP		Stops operation.
DATA SYNC (Rear of Tester)	Any Read	Provides scope sync point during read operations. Signal is positive-going at beginning of data pattern (which follows cylinder byte) and drops at end of track. Because of timing variations and propagation delays between tester, drive, and scope, the first bit of the data pattern may not actually be displayed.

3. If the cylinder and difference are correct, but an address error is indicated, proceed as follows:
   a. Press FAULT. Address Error (Fault bit 8) is stored in drive Fault register. FAULT switch must be pressed to clear that bit.
   b. Select R/W ONLY.
   c. Reread cylinder address.
   d. If ADDRESS VERIFY display matches CYLINDER display, the error is not a positioning error; a read error caused the previous "address error".
4. If CYLINDER and ADDRESS VERIFY cannot be matched, cause of the address error was a positioning error.

While performing sequential forward seeks, and with the TAG LINE SELECT switch set to CYLINDER, the display should be incrementing its binary count.

Seek Operations

1. Set Mode Select switch to desired position.
2. If seeking only is desired, set READ/WRITE switch to neutral (ACC ONLY) position
3. Set INPUT switches as follows:
   a. For direct or continuous seeks, set to desired cylinder.
   b. For sequential forward or reverse seeks, set in seek length. Do not turn on 256 switch or seek lengths other than desired seek lengths will be obtained. For example, if seek of 256 is commanded,access will seek to: 0, 256, 1, 257, 2, 258, 3, 259, and so on.
4. Set REPEAT/SINGLE switch as follows:
   a. In REPEAT, selected seek is continuous until STOP is actuated. Exceptions: only one seek is made if DIRECT is selected; if SEQ REV is selected, seeking stops when cylinder 000 is reached.
   b. In SINGLE, one seek is made for each START switch actuation.
5. Press START to initiate execution.

If CONT and SINGLE are both selected, actuate RESET if the seek address is to be changed. This permits the tester to gate internally the new current address. Otherwise, the tester will command a return seek to the original starting cylinder (stored when the operation first started).

Write Operations

All write routines write from Index-to-Index. Each track has the cylinder address/bit pattern repeated. Proceed as follows:

1. Select head as follows:
   a. Set Mode Select switch to HEAD.
   b. Set INPUT switches to desired head.
   c. Press LOAD.
2. Set READ/WRITE switch to WRITE.
3. Load bit pattern as follows:
   a. Set Mode Select switch to UPPER.
   b. Set INPUT switches (32 through 1) to first (most significant) bits of bit pattern.
   c. Press LOAD. Verify that pattern is displayed by UPPER PATTERN indicators.
   d. Set Mode Select switch to LOWER.
   e. Set INPUT switches (32 through 1) to lower six (least significant) bits of bit pattern.
   f. Press LOAD. Verify that pattern is displayed by LOWER PATTERN indicators.
4. If more than one track is to be written on, select desired seek mode. To format a pack, proceed as follows:
   a. Perform RTZ.
   b. Load desired bit pattern.
   c. Set INPUT switches to 000000001.
   d. Select REPEAT mode.
   e. Set Mode Select to SEQ FWD.
   f. Set LOAD/SEQ HEADS to SEQ HEADS.
   g. Press START. Pattern will be written with head 00 on all tracks. After track 410 has been written, access returns to zero and writes from 0 to 410 with head 01. Sequencing continues through head 18. Operation continues until STOP is selected.
   h. If formatting a pack with only one head, perform all steps except f. (Set LOAD/SEQ HEADS to neutral.)

5. If no seeks are needed, select R/W ONLY.
6. Set REPEAT/SINGLE as follows:
   a. In SINGLE, one seek/write operation is performed for each START. If in R/W ONLY, no seek is performed.
   b. In REPEAT, seek/write operations continue until STOP is actuated. If in R/W ONLY, the same track is continuously rewritten.
7. Press START to initiate execution.

Read Operations

Read operations are primarily track oriented. The tester compares the cylinder address read from the disk with the current cylinder address. If an error occurs, execution stops. Read Gate stays up for the remainder of the track; however, the pattern read from the disk is NOT compared with the loaded pattern. Pattern read errors will therefore not be detected by the tester. Proceed as follows:

1. Select head as follows:
   a. Set Mode Select switch to HEAD.
   b. Set INPUT switches to desired head.
   c. Press LOAD.
2. Set READ/WRITE switch to READ.
3. If it is necessary to observe read waveforms within drive, connect oscilloscope vertical inputs to desired test point. Sync positive on DATA SYNC jack on tester rear panel. Display is initiated at leading edge of first data bit (first bit following cylinder byte). Because of timing variations and propagation delays, first bit may be missed so that display starts at second bit.
4. Set TAG LINE SELECT switch on maintenance panel to ADDRESS VERIFY. Panel indicators then indicate cylinder address read by tester. If performing a repeat read without accessing (R/W ONLY, step 7d), indicators may appear to be blank. This effect is caused because the lamp drivers cannot react fast enough to display data inputs. Display may be obtained by selecting STOP or one of the access/read modes.
5. If more than one track is to be read, select desired seek mode. To verify read capabilities of all heads on all cylinders:
   a. Perform RTZ.
   b. Select REPEAT mode.
   c. Set Mode Select to SEQ FWD.
   d. Set LOAD/SEQ HEADS to SEQ HEADS.
   e. Press START. Cylinder 000, head 00 is read, then cylinder 001, 002, up to cylinder 410. Procedure repeats with cylinder 000, head 01. Head increments automatically through cylinder 410, head 18. Operation continues until STOP is selected.
6. To read one track (no seeks), select:
   a. Desired head.
   b. R/W ONLY.
   c. REPEAT.
   d. START. Entire track is continuously read.

SECTION 3

THEORY OF OPERATION

INTRODUCTION

Theory of operation for the drive is organized into two parts. The first part describes the major mechanical assemblies. The second part describes the logical functions and the signals exchanged with the controller.

Functional descriptions are frequently accompanied by simplified logic diagrams. These diagrams are useful both for instructional purposes and as an aid in troubleshooting. Figure 3-1 illustrates the logic symbology used by the illustrations in this manual. The diagrams have been simplified to illustrate the principles of operation; therefore, other elements may be omitted. The logic diagrams in the Maintenance manual should take precedence over the diagrams in this section whenever there is a conflict between the two types of diagrams.

The descriptions are limited to drive operations only. In addition, they explain typical operations and do not list variations or unusual conditions resulting from unique system hardware or software environments. Personnel using this manual should already be familiar with principles of operation of the computer system, the controller, programming considerations (including the correct sequencing of I/O commands and signals), and track format (i.e., data records and field organization).

ASSEMBLIES

Refer to Section 1 for major assembly locations.

POWER SUPPLY

Each drive cabinet has a self-contained power supply accessible by swinging open the logic chassis. The power supply is contained in two locations. The ac portion of the supply, consisting of transformers, rectifiers, triacs, and line filters, is mounted in the lower rear of the drive cabinet. The dc portion of the supply, consisting of rectifiers and filters and the relays for power sequencing, is mounted in the lower portion of the logic chassis. Power supply cooling is accomplished by room air for the ac portion. In S/C 07 with PE35350A and above, the blower system also provides cooling air to the power supply. For the dc portion, cooling air is blown over the chassis from a blower at the front of the drive cabinet.

The power supply has the following outputs:

1. +20Y for power sequencing control.
2. ±20 vdc used by the logic.
3. ±9.7 vdc which, in turn, is regulated to ±5 vdc in the logic chassis.
4. ±46 vdc for the voice coil positioner.
5. -16 vdc to retract the carriage under emergency conditions.

Power distribution and sequencing control are illustrated in Figures 3-2 through 3-4.

AC/DC Distribution

Input power is made available to the power supply via the closed contacts of the UNIT POWER circuit breaker. With this breaker closed, the blower motor operates. AC power is available to the remainder of the circuit breakers.

The remainder of the ac distribution occurs when the input voltage is applied to transformer A1T3. An ac voltage of about 24 volts is picked off the secondary of T3 and applied to the First Seek Interlock (brush motor in older units) but application of the voltage to the motor does not occur until the spindle motor is started. Another T3 output is rectified to +22 volts (+20Y), which is used as a control voltage within the power system.

With +20Y available, sequence power is enabled. Solid state switches A1Q1 through A1Q4 effectively operate as ac relays enabled by +20Y inputs.

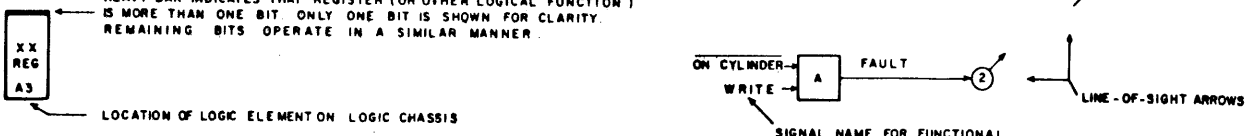
The input applied to pin 1 of these devices is transferred to output pin 2 only if pin 3 has +20Y on it while pin 4 is grounded. These enables are described in detail in the Power Up Sequence discussion.

GENERAL INFORMATION

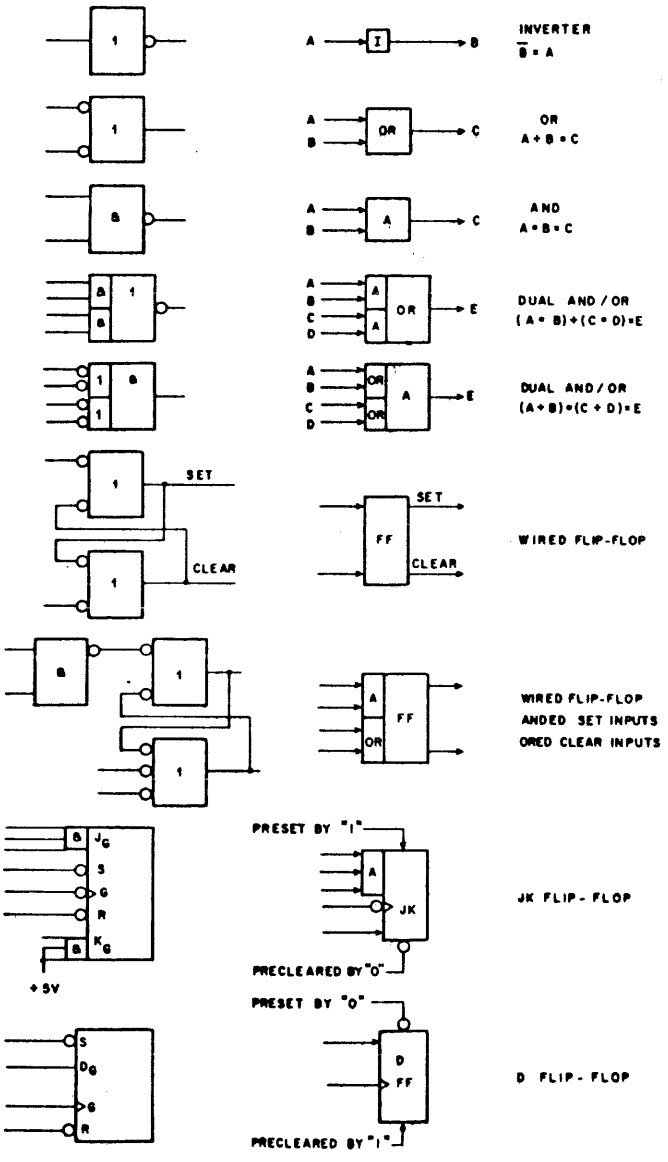
SIMPLIFIED DIAGRAMS IN THIS MANUAL SHOW THE FUNCTIONAL FLOW OF SIGNALS THROUGH THE DRIVE. THE DIAGRAMS HAVE BEEN SIMPLIFIED TO SERVE AS A GUIDE IN TROUBLESHOOTING AND IN UNDERSTANDING DRIVE OPERATIONS. REFER TO THE COMPLETE LOGIC DIAGRAMS FOR ACTUAL TEST POINTS AND SIGNAL LEVELS.

ALL LOGIC IS SHOWN ON POSITIVE LOGIC REPRESENTATION. SIGNAL LEVELS ARE DISREGARDED. ALL SIGNALS ARE NAMED WHEN THE FUNCTION TO BE ACCOMPLISHED REQUIRES A LOGICAL 1, REGARDLESS OF ACTUAL SIGNAL VOLTAGE LEVEL.

SYMBOLS



LOGIC SYMBOLOGY CONVERSION



FLIP-FLOP OPERATION

WIRED FF

FF OUTPUTS ARE COMPLEMENTARY UNLESS BOTH INPUTS RECEIVE SIMULTANEOUS ENABLES. IF SO, BOTH OUTPUTS ARE HIGH ("1").

JK FF

JK FF IS ENABLED (TO CHANGE STATE) BY DYNAMIC TOGGLE. IF CIRCLE IS SHOWN AT TOGGLE, CIRCUIT IS ENABLED BY NEGATIVE-GOING TOGGLE ("1" → "0"). PRESETS AND PRECLEARS DO NOT REQUIRE TOGGLE TO CHANGE STATE.

JK TRUTH TABLE

J	K	BEFORE TOGGLE		AFTER TOGGLE	
		SET	CLEAR	SET	CLEAR
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

D FF

SAME AS JK, EXCEPT THAT THERE IS NO DATA INPUT TO CLEAR SIDE. FF SETS ONLY IF D INPUT IS "1" WHEN TOGGLE GOES TO "1". IF D INPUT IS "0" AT TOGGLE, FF CLEARS.

7M7

Figure 3-1. Simplified Logic Symbology

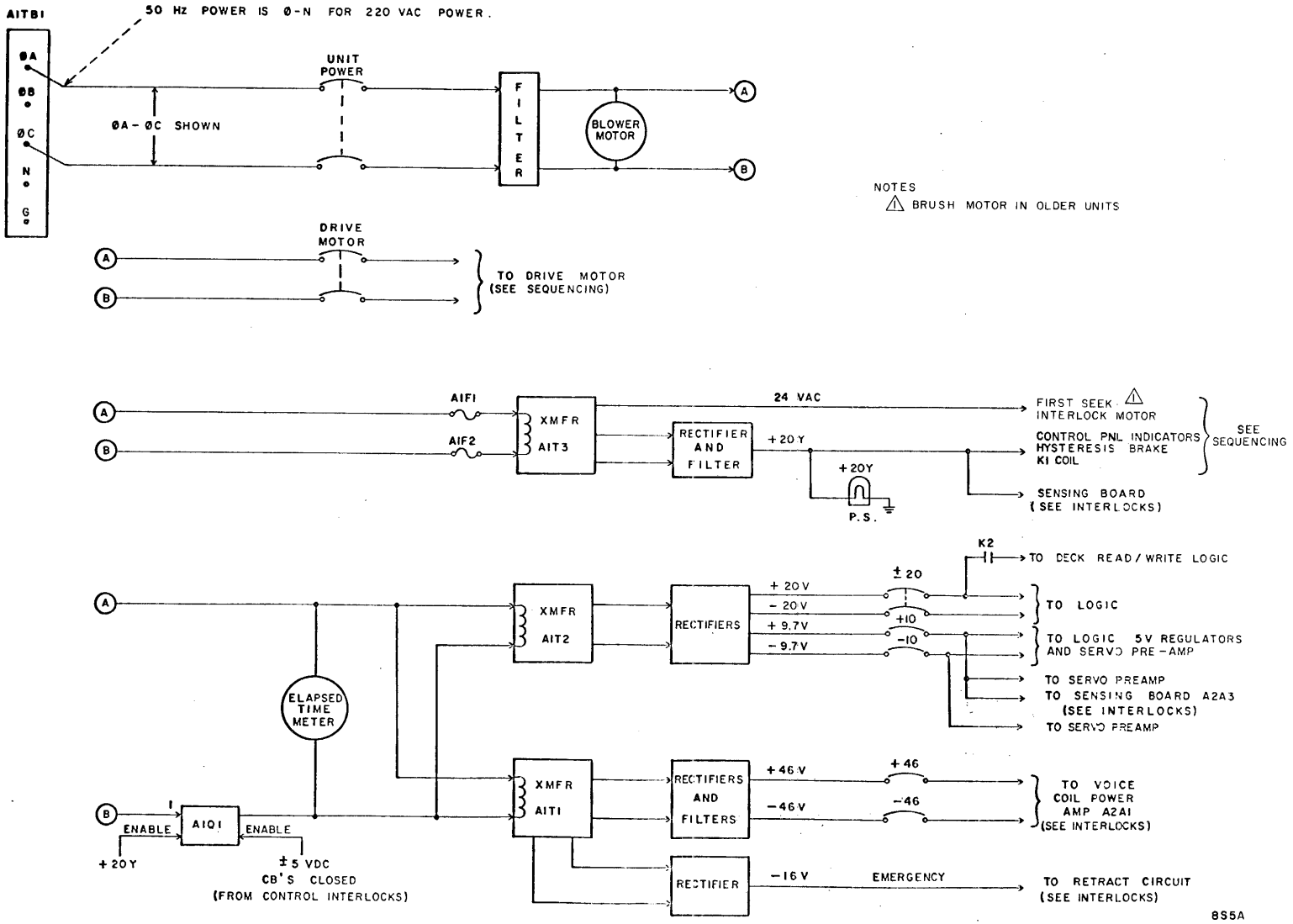


Figure 3-2. Power Distribution

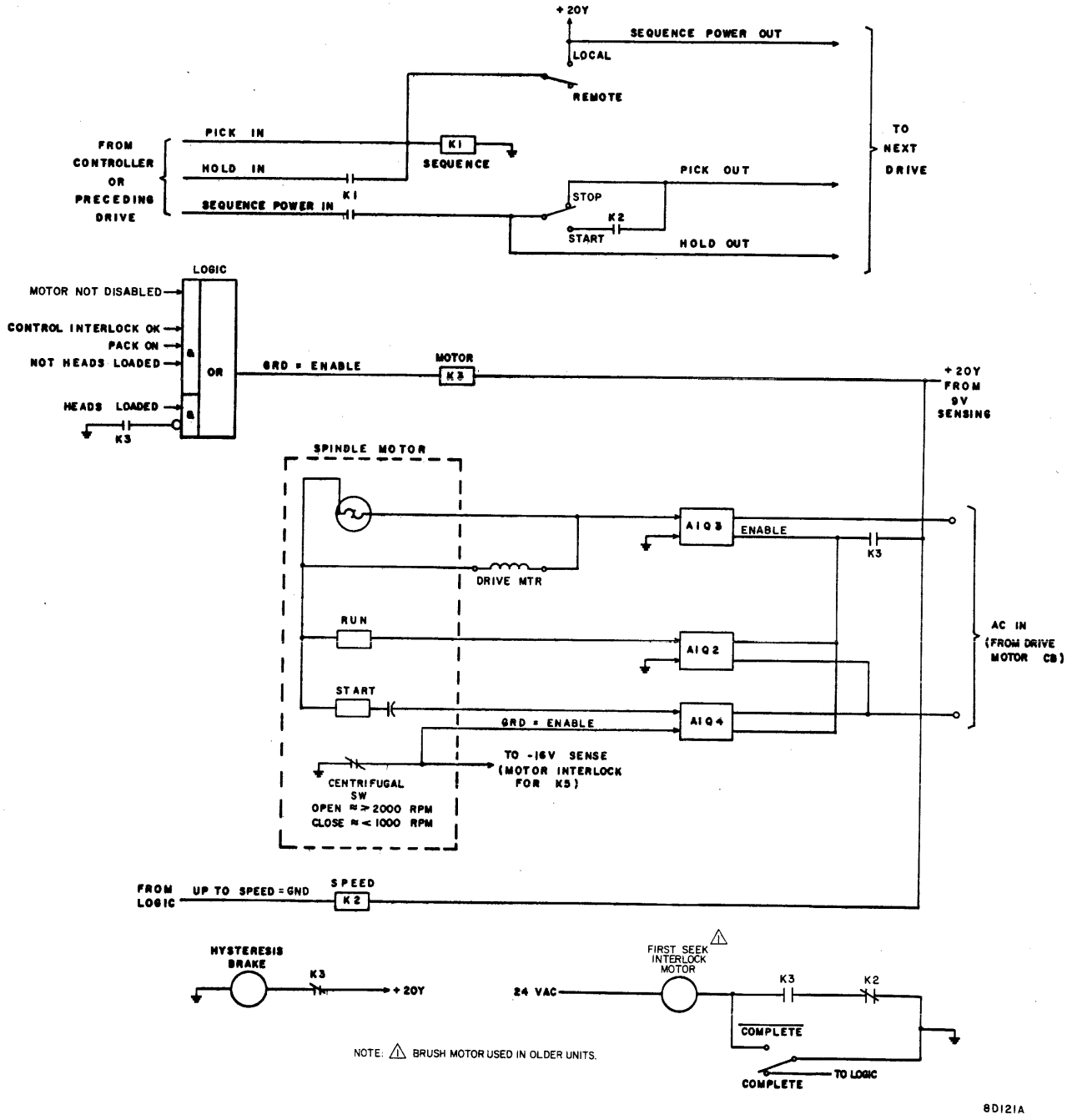


Figure 3-3. Power Sequencing

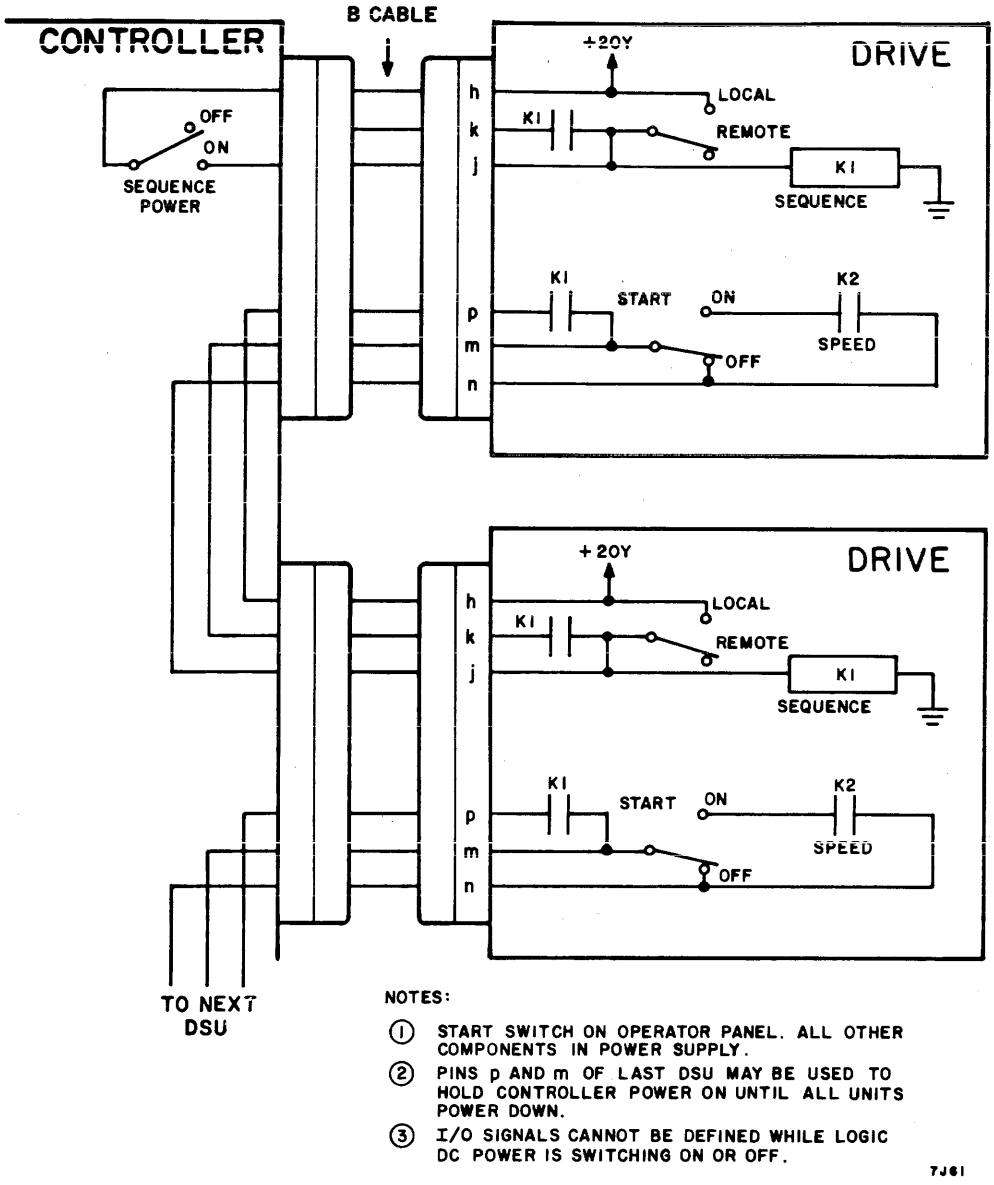


Figure 3-4. System Power Sequence Lines

With A1Q1 enabled, ac is applied to transformers A1T1 and T2. In the case of T2, four distributative voltages developed across the secondary windings are applied to rectifier/filter circuits. The four circuits (+9.7, -9.7, +20, and -20 vdc) are not adjustable and incorporate no switching device other than circuit breakers for circuit protection. Both polarities of the 9.7 volt circuit are voltage level regulated and made adjustable to ±5 vdc in the DC power panel.

The voltages developed across A1T1 are applied to rectifier and filter circuits. None of the voltages are adjustable. The actuator power (±46 vdc) incorporates no switching devices other than circuit breakers for protection. The emergency retract power (-16 vdc) uses retract relay K5 to connect or disconnect the emergency retract capacitor to the voice coil. This function is explained further in the Emergency Retract discussion.

Overtemperature Monitoring

An airflow actuated switch is mounted in the DC power supply, at the bottom of the logic chassis. Loss of cooling air (excessive temperature) causes the switch to close and the TEMP indicator on the control panel to light.

A high temperature condition has no effect on unit operation.

The logic temperature switch is kept open by normal air flow from the cooling blower. Low air flow allows the switch to close.

Power On Sequence

Power application to a unit is sequenced by logic and by relays in the power supply. Refer to Figure 3-3 and 3-4. Assume that all circuit breakers are closed. If so, the blower motor is operating and the hysteresis brake is energized by +20Y.

Power on may be controlled either by the controller (remote) or locally for maintenance purposes (local). The Power On Sequence is as follows:

1. +20Y is connected to relay K1 either by placing the LOCAL/REMOTE switch in the LOCAL position or, in the REMOTE position, from the controller. (K1 contacts are in the switch circuit so that, once the unit is powered up, the LOCAL/REMOTE switch can be switched without dropping power, assuming ground is available from the controller.) Other contacts of K1 enable solid state switch A1Q1 to turn on the elapsed time meter and to bring up dc power.
   a. If the START switch is not on in the first unit, Sequence Power Out in the second drive has a continuous path through Sequence Power In, K1 (first drive) START switch, Pick Out (first drive) to Pick In (second drive) to energize its K1. In turn, Hold In applies a holding current to the second drive's K1. This process continues through the remainder of the drives until one is encountered with the START switch on.
   b. For the remainder of the sequence, assume that the first drive has a disk pack installed, that all interlocks are closed, and that the START switch is on. Power cannot be sequenced to the next drive until speed relay K2 closes.
2. Because all interlocks are closed (Figure 3-5) and with +20Y power available, the START indicator is lighted. Now that K1 is closed, the control interlock signal provides the last enable (Figure 3-3) to energize Motor relay K3.
3. The closed contacts of K3 cause the following:
   a. +20Y enables solid state switches A1Q2, A1Q3, and A1Q4. These switches can now conduct ac power to the spindle motor.
   b. Because the motor is stopped, the centrifugal switch inside the motor is closed. This provides a ground enable to A1Q4 to connect the start winding and capacitor to ac power. At 2000 rpm the switch transfers to open, disconnecting the start winding and enabling the run winding.
   c. Apply GND to the First Seek Interlock cycle (brush motor in older units). The First Seek Interlock cycle (brush cycle in older units) transfers to the not complete (in progress) position.
   d. Removes power from the hysteresis brake.
4. When the logic determines that the spindle speed exceeds 3000 rpm, speed relay K2 energizes.

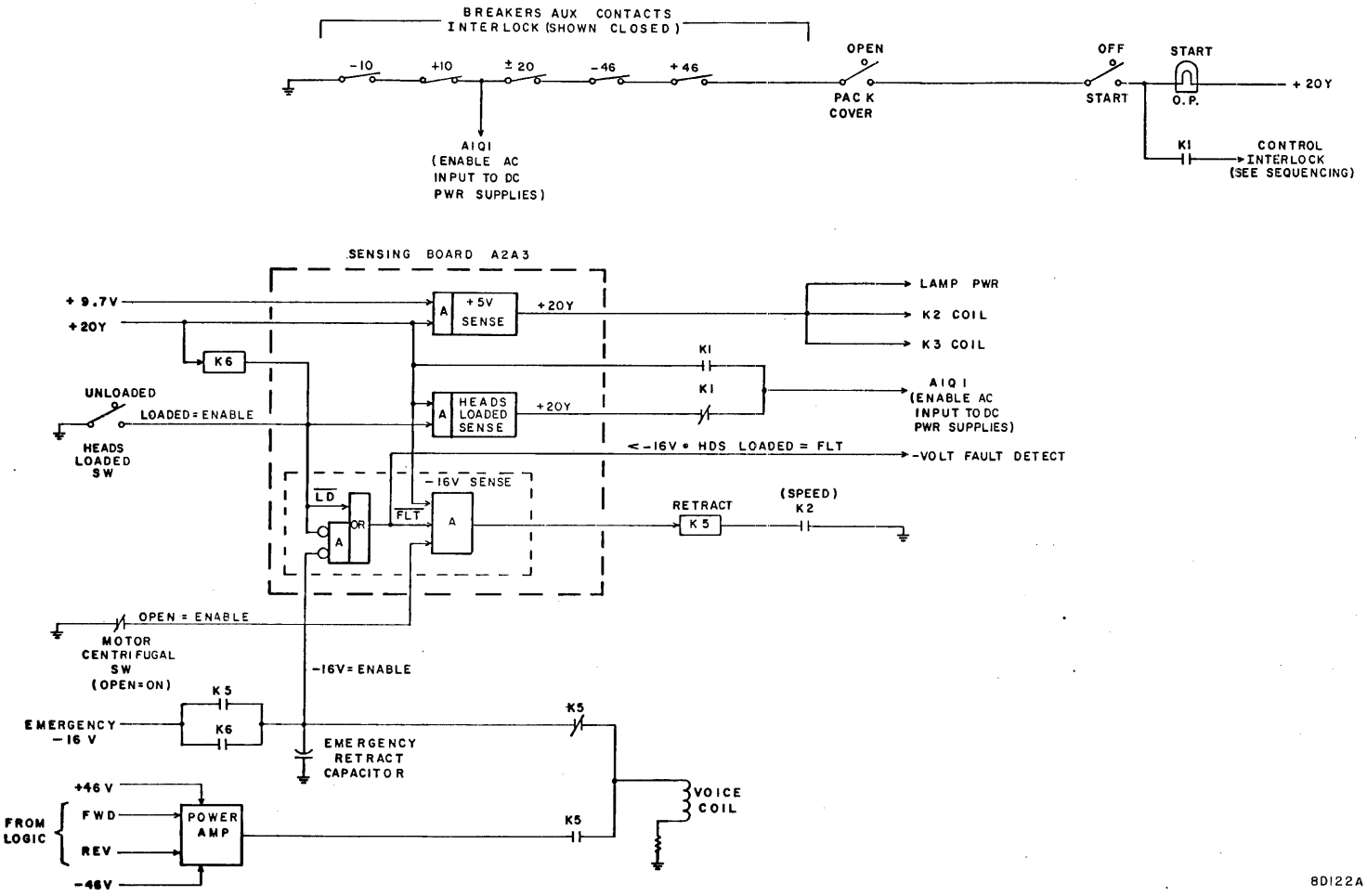


Figure 3-5. Power Interlocks

5. With relay K2 closed:

   a. +20 vdc distributed to the read/write logic (Figure 3-2).

   b. One of two grounds removed to the brush motor (Figure 3-3).

   c. +20Y sequence power routed to next drive via the controller.

   d. Retract relay K5 energized (Figure 3-4).

6. The transferring contacts of K5 cause the following:

   a. Disconnects the emergency retract capacitor from the voice coil while connecting it to the -16v power supply to allow it to charge to -16 volts. This capacitor then functions as a charged battery (with no current drain) to store the retracted energy required under all conditions.

   b. Connects the power amplifier A2A1 to the positioner so that the logic may control the positioner.

7. The First Seek Interlock cycle starts before the pack reaches speed. In older units the disk pack cleaning brushes sweep the disk surfaces before the pack reaches speed. The brush cycle switch mechanically transfers to the complete position upon completion of the brush motor revolution (15 seconds). This removes the remaining ground to the brush motor to disable it. It also signals load heads to the logic.

8. Completion of the interlock cycle (brush cycle in older units) allows the start of the First Seek (load heads) function. The logic commands the positioner to move the carriage forward. Refer to the First Seek discussion for further information.

9. When the heads move onto the pack, the heads loaded switch closes. This causes the following:

   a. Provides a control signal to the logic for further loading/unloading sequencing.

   b. Maintains a Motor relay K3 enable so that the motor continues to operate if the control interlock opens. This prevents the motor from being shut down until the heads are unloaded.

   c. Energizes relay K6. If any condition occurs where Retract relay K5 opens, K6 continues to apply -16v retract voltage to the voice coil until the heads unload.

   d. Enables the -16v Sense circuit. If the -16v power becomes insufficient (loss of power), the Fault FF is set and Retract relay K5 opens. Relay K5 connects the retract voltage to the voice coil while removing logic control of the voice coil.

Emergency Retract and Data Protection

Certain emergency conditions could occur which require immediate disabling of the write circuits and full retraction of the heads. These conditions are:

1. Loss of ac power, either site power or UNIT POWER circuit breaker.
2. Opening of any of the control interlocks (Figure 3-5).
3. Overheating of spindle motor. If this occurs, the spindle motor thermostat (Figure 3-3) opens: this applies ac across the DRIVE MOTOR circuit breaker coil to open the contacts. Loss of speed (step 4) occurs.
4. Loss of spindle motor speed.
5. Loss of any of the following dc voltages: +20Y, +9.7, or -16.

If any of these conditions occur, the read/write logic is disabled and the heads are unloaded. Refer to Figure 3-7 for timing of these conditions.

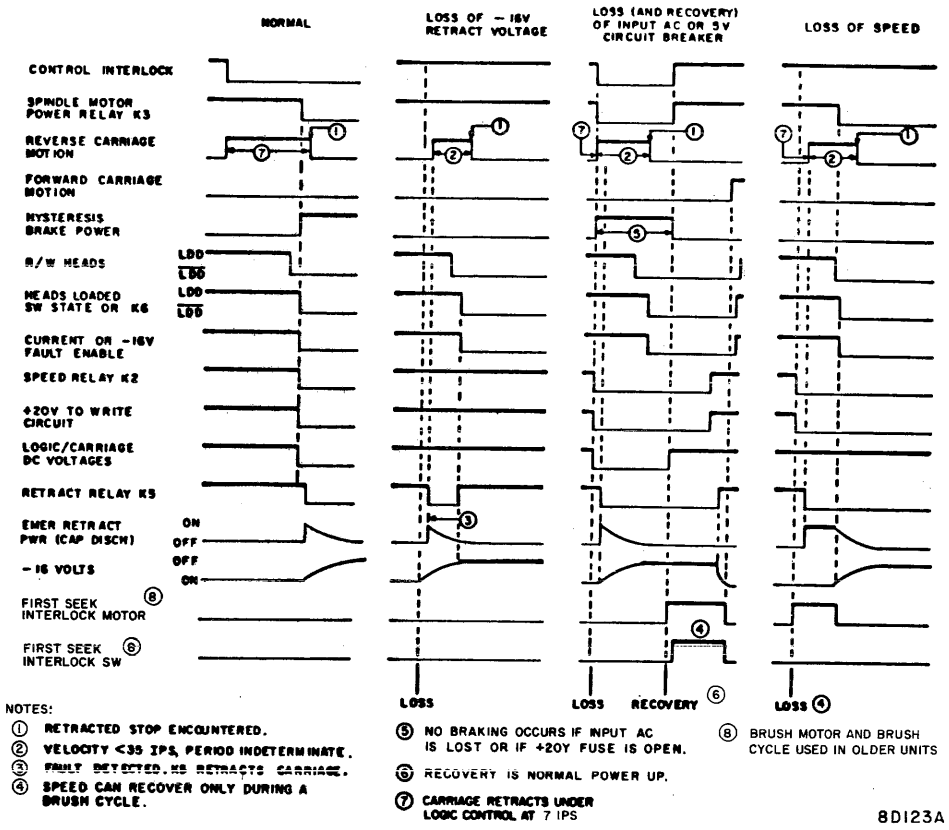


Figure 3-6. Power Off Timing

Loss of AC Power

The following events occur upon catastrophic loss of the ac power or opening of either 5v circuit breaker:

1. All dc power supplies begin dropping their outputs to zero and the logic is disabled by low voltage fault detection circuits.

A Fault sets the Fault FF to light the FAULT indicator. Heads cannot be reloaded until the condition is cleared. The +20 volt write power is lost if Speed relay K2 opens due to any of the following emergency conditions.

2. +9v Sensing detects that +9v is dropping disabling lamps and relays K2 and K3. Relay K2 opens disabling K5 relay.

3. With K2 open, +20 vdc is removed from the read/write logic protecting the data or the pack.

4. With K5 open, the normally-closed contacts of K5 (Figure 3-5) provide a path from the emergency retract capacitor A2C2 to the voice coil. This negative voltage pulls the carriage back to its retracted stop.

Control Interlock Opening

If the control interlock (Figure 3-5) opens, the heads unload normally as explained in Power Off Sequence. Pressing START to extinguish the indicator opens the interlock to initiate the normal unload heads sequence. There are certain special emergency sensing conditions:

1. If either the +10 or -10 circuit breaker opens, all ac power input to the logic and voice coil power supply is opened. A1Q1 (Figure 3-2) is disabled. The effect is the same as if all ac power is lost.

2. Opening the 20v circuit breaker generates an undervoltage condition to set the Fault FF. The control interlock opens but the heads do not unload because the loss of -20v provides no power for a normal retract and a seek error will occur. The motor will not stop as long as the heads are loaded.

3. Opening of any dc circuit breaker or interlock breaks the control interlock. If -46v breaker opens, no voltage is available for normal retract and the motor will not stop as long as the heads are loaded.

All of these conditions extinguish the START indicator. Any undervoltage condition (±20v or ±5v) sets the Fault FF.

Loss of Speed

If the spindle motor speed drops below 2700 rpm, the following events occur:

1. The speed detection circuit in the logic detects the speed loss and opens Speed relay K2. As a backup circuit, when the speed is less than about 2000 rpm, the motor centrifugal switch closes. This breaks the gate in the -16v sense circuit (Figure 3-5) to open K5.

2. With K2 open:

   a. K5 opens to apply -16v retract voltage to the voice coil.

   b. +20 vdc power is removed from the read/write logic to protect data by initiating writing. Loss of on cylinder also inhibits write gate.

3. The speed loss sets the Motor Disable latch and generates an Unload Heads signal to initiate a normal unload heads until emergency retract takes command.

4. Relay K6 remains energized to continue to apply -16v retract voltage until the heads retract sufficiently to open the heads loaded switch.

5. When the heads unload:

   a. Unit Ready drops.

   b. Relay K3 opens to shut down the spindle motor and to disable the First Seek Interlock motor (brush motor in older units).

Loss of DC Power

If +20Y power is lost, all relays open and the ac input to A1T1 and A1T2 transformers open. The effect is the same as if all ac power were lost.

If +9.7v is insufficient, the following occur:

1. Relays K2 and K3 are opened by the +9v Sense circuit.
2. With K2 open:
   a. K5 opens to apply -16v retract power.
   b. +20v power removed from read/write chassis.
3. With K3 open:
   a. The spindle motor is disabled.
   b. The hysteresis brake is energized.
4. In addition, the undervoltage condition will set the Fault FF in the logic; the FAULT indicator lights. The condition must be reset to load heads again.

If -16v power is lost, the following occur:

1. The -16v Sense circuit opens K5. It also generates an undervoltage fault condition to set the Fault FF.
2. With K5 open, retract power is applied to the voice coil. Since the undervoltage fault has disabled the read/write logic, the circuit is disabled prior to carriage retraction.
3. Relay K5 energizes when the heads unload. Heads cannot load until the FAULT indicator is cleared.

If ±20v or ±5v power becomes insufficient, the heads do not retract. However, the undervoltage condition sets the Fault FF. This has the following effects:

1. FAULT indicator lights.
2. If heads are not loaded, loading is inhibited.
3. All controller-initiated seeks are inhibited.
4. Read, Write, and Erase gates are inhibited.
5. Bit 1 (Pack Unsafe) is up during a Read Control Status tag.
6. During a Read Fault Status tag the following bits are up:
   a. Bit 3 (+volt) for +20v or +5v fault.
   b. Bit 4 (-volt) for -5v or -20v fault.

Power Off Sequence

The normal Power Off sequence begins when the controller opens the sequence power line to the drive. Sequencing is then as follows (see Figures 3-6 and 3-7):

1. Relay K1 de-energizes:
   a. The control interlock opens to raise an Unload Heads command within the logic. This sets the RTZ latch which, in turn, causes the carriage to retract at 7 ips. The carriage performs a normal RTZS, except that the logic that normally stops the carriage at cylinder 000 is inhibited.
   b. Sequence power is dropped to the next drive.
   c. Power stays up within the drive because the heads loaded sense function of sensing board A2A3 (Figure 3-5) enables A1Q1 as long as the heads remain loaded.
2. When the heads unload:
   a. Relay K3 de-energizes.
   b. The speed detection circuit is disabled to de-energize relay K2.
   c. Unit Ready drops.
   d. If power is dropped by the system (K1 open), ac power is removed from the dc power supplies. If power is dropped because START was turned off, however, dc power is not dropped.
3. With K3 open:
   a. The spindle motor is disabled.
   b. Power is applied to the hysteresis brake.
4. With K2 open:
   a. +20v removed from read/write logic.

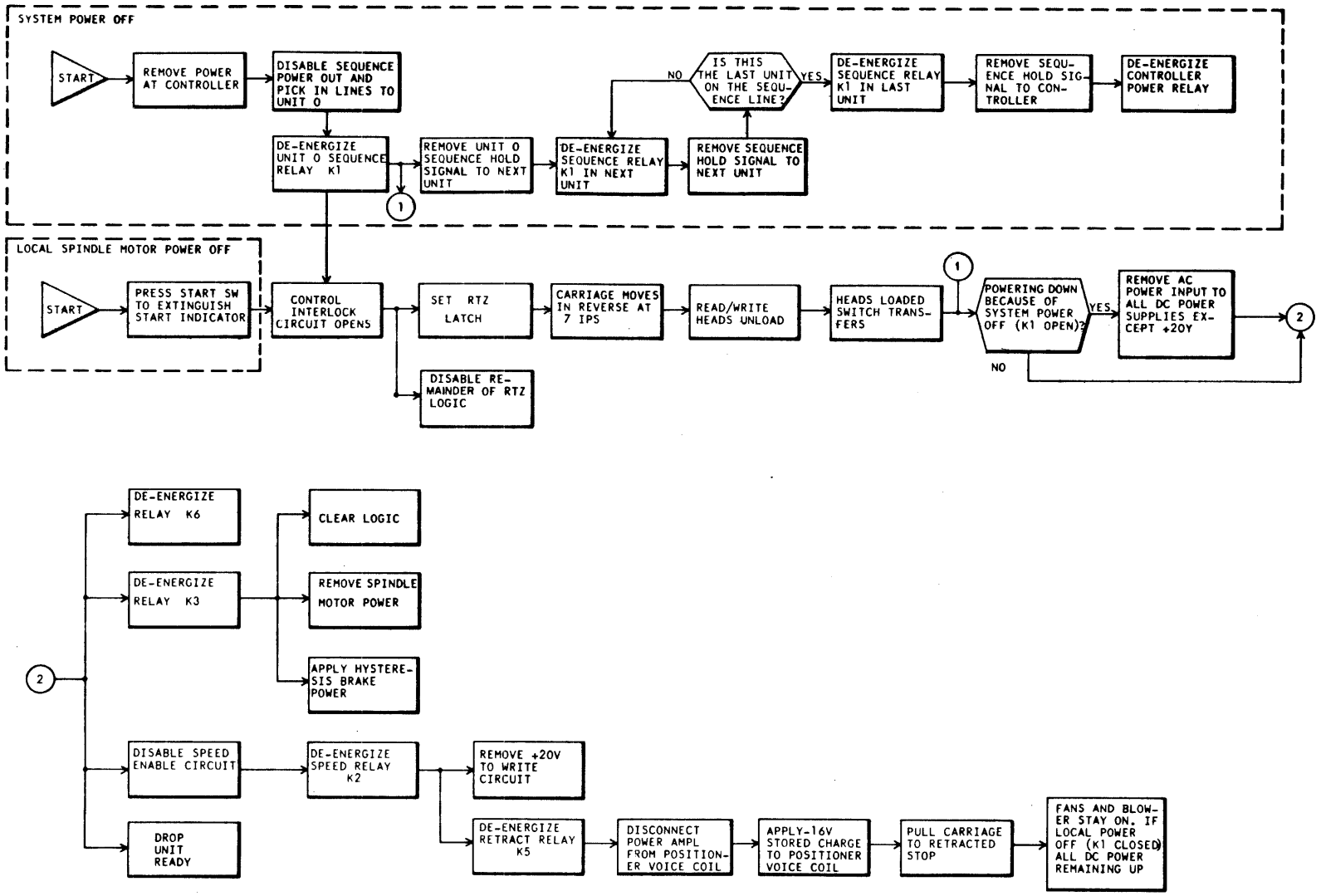


Figure 3-7. Power Off Sequencing

b. Relay K5 opens. The emergency retract capacitor discharges through the voice coil to pull it back against its retracted stop.

Assuming K1 is open, and with the heads retracted, the +20Y enable is removed from A1Q1 to disable the primaries of T1 and T2. The only dc voltage remaining on is the +20Y required to power up again.

LOGIC CHASSIS

The logic chassis assembly consists of a wire wrap board, logic cards, test point panel, air plenum and dc power supply. The entire assembly forms the rear door to the cabinet. Flexible tubing from the blower assembly connects to the air plenum and provides air to cool the logic cards and the dc power supply.

Some cards span two rows and are referred to as full-size cards. Other span a single row and are called half-size cards. Refer to the Diagrams section of the Maintenance manual for a description of the logical functions performed by the cards. The Logic Card manual provides a physical description of the cards. The Wire Lists section of the Maintenance manual contains a tabulation of the wire wrap connections made in the chassis.

The test point panel at the top of the logic chassis provides a convenient point to measure the dc voltage. At the bottom of the logic chassis assembly, and on the front panel of the dc voltage section of the power supply, are located the LOCAL/REMOTE switch, the indicator for +20Y power and the circuit breakers for ±46v, ±20v, and ±10v. Specific information on each control or indicator on the test point and dc power panel is provided in the Operation section of this manual.

Deck Assembly

The deck assembly mechanism (Figure 3-8) drives the disk pack and loads and positions the read/write and servo heads. The deck assembly consists of a drive motor, hysteresis brake, spindle, actuator, two transducers, and a first seek interlock assembly (disk cleaner assembly in older units).

Drive Motor Assembly

The drive motor drives the spindle assembly. The motor is a 3/4-hp unit of the induction type. The motor is secured to a mounting plate. The motor mounting plate is secured to the underside of the deck plate in such a manner as to allow control of belt tension. Power is transferred to the spindle via a flat, smooth-surfaced belt that threads over the pulleys of the spindle and drive motor. An idler spring maintains a constant tension on the motor mounting plate to keep the belt tight.

A second pulley on the drive motor shaft links the motor (via a V-belt) to the hysteresis brake.

The temperature of the drive motor is monitored by an internal thermostat. If the motor overheats, the thermostat opens. This applies ac across the DRIVE MOTOR circuit breaker coil to open the contacts. The result is a speed loss (refer to Power Supplies). The DRIVE MOTOR circuit breaker must be reset to ON to restore operation.

Hysteresis Brake Assembly

The hysteresis brake decelerates the drive motor during a Power-Off sequence (refer to Power-Off sequence paragraph). The brake is energized whenever Motor relay K3 is de-energized. On units with S/C 11 and below the hysteresis brake mounts on a plate which, in turn is mounted on the motor mounting plate; and the brake and motor shafts are linked via a V-belt and a pulley on each shaft. On units with S/C 12 and above the hysteresis brake is attached to the drive motor housing and the motor and brake are coupled on a flexible coupling.

The brake consists of two concentric permeable bodies. These cylinders are assembled, one inside the other, with a uniform gap separating the outer diameter of one from the inner diameter of the other. These adjacent surfaces are machined to contain a series of pole faces. A permanent magnet, in the shape of a cup, fits in the gap to separate the cylinders. The cup is connected to the brake

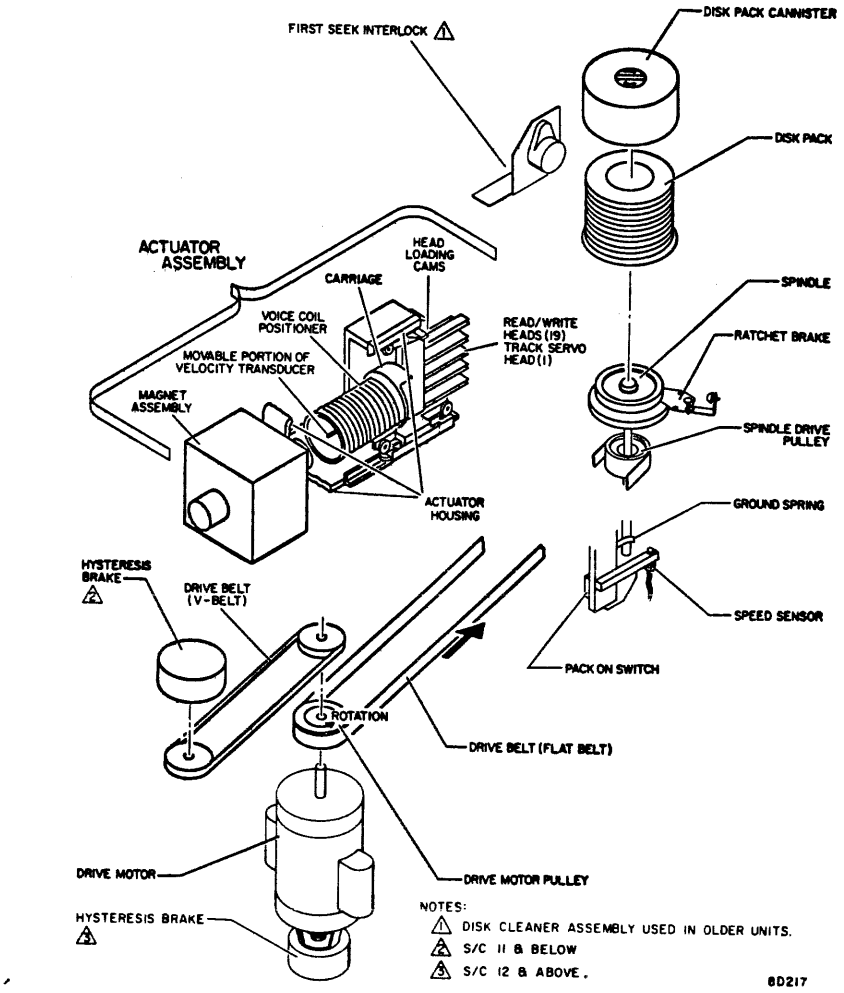


Figure 3-8. Deck Assembly

shaft. As long as spindle motor power is applied, brake power is not available and the cup is driven at the speed of the motor. When spindle motor power is removed, braking power is applied. A flux field is created between the inner and outer cylinder pole faces as braking voltage (+20 volts) is applied to the inner cylinder. The flux field sets up what is in effect magnetic friction between the inner cylinder and the cup, causing the cup (and brake shaft) to decelerate. Brake deceleration in turn causes spindle motor deceleration.

Spindle Assembly

The spindle assembly is the physical interface between a drive and a disk pack. The surface of the pack mounting plate (Figure 3-9) mates directly with the center of the disk pack.

A vertically free-floating lockshaft runs through the center of the spindle assembly. The upper end of the lockshaft contains internal threads that engage the external threads of a stud projecting from the

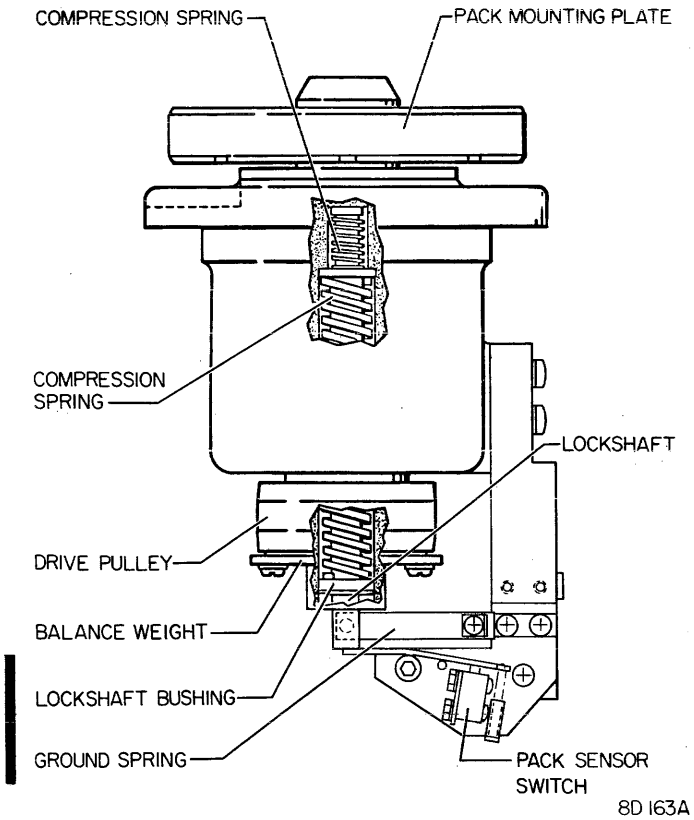


Figure 3-9. Spindle Assembly

disk pack. When the disk pack canister cover handle is rotated clockwise, the spring-loaded lockshaft is pulled upward and the disk pack is pulled down. As a result, the mating surfaces of the disk pack and spindle are engaged by a force of approximately 325 pounds. When the disk pack is fully engaged, a release mechanism in the canister handle frees the canister from the disk pack.

The spindle is locked by the pack canister when installing or removing a disk pack. This makes it easier to install or remove a disk pack by preventing spindle rotation.

The spindle is driven by a flat belt linking the spindle drive pulley to the drive motor pulley.

The pack sensor and ground spring (Figure 3-9) are mounted at the lower end of the spindle assembly. The ground spring is mounted so that it is always in contact with the lockshaft to bleed off any accumulation of static electricity on the spindle to the deck through a ground strap. The pack sensor contacts transfer in response to the vertical movement of the lockshaft. When the shaft is up (disk pack mounted), the contacts are closed. When a pack is not installed, the shaft moves downward to deflect the switch actuator and transfer the contacts. The switch is part of the interlock that inhibits spindle motor power to an improperly configured unit.

Actuator

The actuator consists of the carriage, actuator housing, and magnet assembly. The actuator (Figure 3-10) is the device that supports and moves the read/write and track servo heads. The forward and reverse moves of the carriage on the carriage track are controlled by a servo signal. The basic signal is developed in the logic section and processed by a power amplifying stage in the power supply. The power amplifier output is applied to the voice coil positioner (part of carriage). The signal causes a magnetic field about the voice coil positioner. This magnetic field reacts with the permanent magnetic field existing around the magnet assembly. The reaction either draws the voice coil into the permanent magnet field or forces it away. Signal polarity determines the direction of motion, while signal amplitude controls the acceleration of the motion.

The voice coil positioner is a bobbin-wound coil that is free to slide in and out of the forward face of the magnet assembly. Fastened to the positioner is a head/arm receiver which holds the 19 read/write heads and the single track servo head. The head/arm receiver mounts on the carriage and bearing assembly that moves along the carriage track on eight bearing type rollers. Movement of the positioner in or out of the magnet causes the same motion to be imparted to the entire carriage assembly. This linear motion is the basis for positioning the read/write and track servo heads to a particular track of data on the disk pack. (Refer to Head Loading paragraph for detailed information on read/write head loading and unloading.)

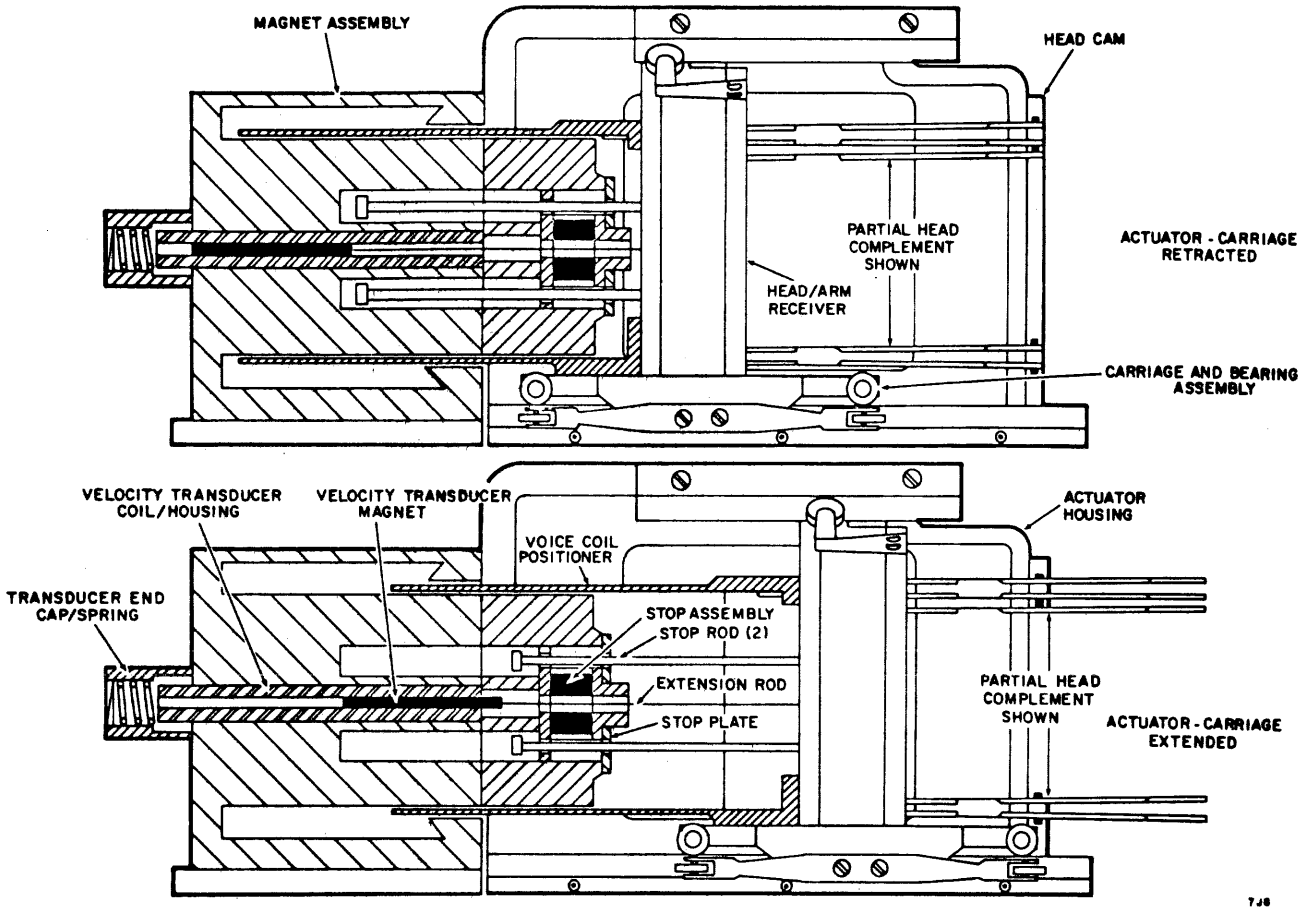


Figure 3-10. Actuator Assembly Elements

The positioning signal is derived in the logic chassis and power supply. The signal is applied to the voice coil positioner via two flexible, insulated, metal straps, the ends of which are secured to the cam mount and the carriage and bearing assembly.

During any Seek operation, the logic must be informed of the current location and velocity of the carriage. This information is provided by the velocity transducer in the magnet assembly and the lone track servo head installed on the head/arm receiver. The transducer is a two-piece device, one piece stationary and the other movable. Refer to the Transducers paragraph for a complete description.

The actuator contains a stop mechanism to limit extremes in forward and reverse movement. The stop assembly is a rubber cylinder sandwiched between two metal plates. If the carriage moves too far toward the disk pack, the stop rod heads contact the plate on the magnet-side of the rubber cylinder. If the carriage is retracted far enough away from the disk pack, the rear of the head/arm receiver contacts the stop assembly stud protruding through the stop plate.

Head Loading

The read/write heads must be loaded to the disk surfaces before exchanging data with the controller. The heads must be removed (unloaded) from this

position and driven clear of the disk pack either when power is removed from the unit or when the disk pack velocity falls below about 2700 rpm. The actuator components involved in these operations are identified in Figure 3-11.

Head loading amounts to allowing spring pressure of the floating arm (part of head/arm assembly) to move the aerodynamically shaped head face toward the related disk surface. When the cushion of air that exists on the surface of the spinning disk is encountered, it resists any further approach by the head. Spring pressure is designed to just equal the opposing cushion pressure (function of disk pack rpm) at the required height. As a result, the head flies. However, if the spring pressure exceeds the cushion pressure (as would happen if the disk pack lost enough speed), the head stops flying and contacts the disk surface. This could cause damage to the head as well as the disk surface.

To prevent damage to the heads and/or the disk pack during automatic operation, loading occurs only after the disk pack is up to speed and the heads are over the disk surfaces. For the same reason, the heads unload automatically and are retracted if the disk pack rpm drops out of tolerance. During manual operations, heads should never be loaded on a disk pack that is not rotating. Head loading is part of the Power On/First Seek function. As power to the deck is sequenced up, the drive motor starts. This initiates disk pack rotation and a First Seek Interlock cycle (disk cleaning in older units). In older units actual cleaning time is approximately five seconds; total cycle time is 15 seconds.

When the disk pack rpm reaches 3000, the power supply speed relay energizes to establish the ability to continue the operation. Upon completion of the First Seek Interlock cycle (in older units the disk cleaning cycle, brush clear of disk pack), the logic specifies a forward seek and the carriage moves forward toward track 0. Head loading occurs during this forward motion. The carriage continues toward the spindle until the servo detects track 0.

The floating arm (Figure 3-11) is designed to maintain a constant loading force. While the heads are retracted, head cams on the actuator housing bear against the floating arm cam surfaces. The cams

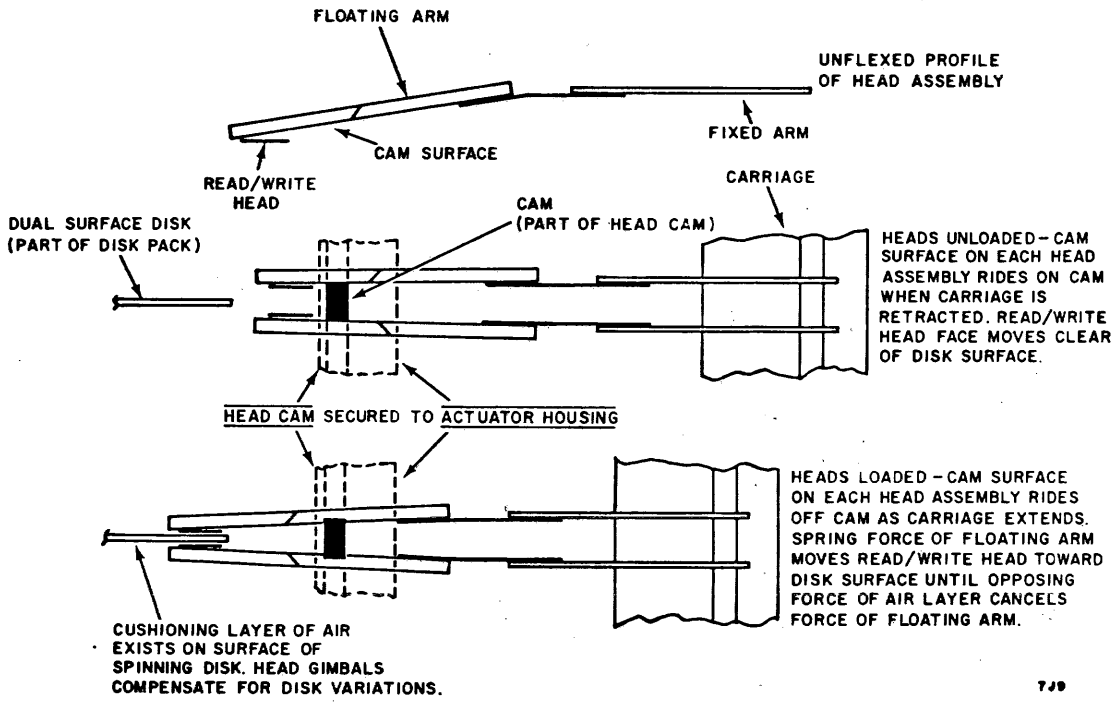


Figure 3-11. Head Loading

support the loading force and hold the heads in unloaded position. As the carriage moves forward, the floating arm cam surface rides off the head cam just after the read/write heads move out over the disk surface. The loading force moves the head face toward the air layer on the surface of the spinning disk until the opposing forces balance.

The heads loaded switch status reflects the state of the read/write heads (loaded or unloaded). This status is used in the logic chassis and power supply. The switch mounts on the carriage track and is transferred by carriage motion. Whenever the carriage is fully retracted, the switch state reflects the unloaded status of the heads. As the carriage moves forward during a Power On/First Seek, the switch transfers at a point within about 0.1 to 0.2 inch forward of the retracted stop. This switch status remains unchanged until the carriage is retracted to the same position and, as such, does not precisely indicate the loaded/unloaded status of the heads. Precise status is determined by the logic when the servo track head senses dibits.

Head unloading occurs whenever power to the unit is removed or disk pack rpm drops below tolerance. Either event drops a speed enable signal to the logic. This causes the voice coil to drive the carriage in reverse from its current location toward the retracted stop. (Either normal or emergency methods can be used. Refer to Power Off Sequence paragraph for additional information.) As the carriage retracts, the cam surfaces encounter the head arms and each head rides vertically away from the related disk surface. The carriage continues back to the retracted position and stops.

Head/Arm Assemblies

Twenty head/arm assemblies are mounted on the carriage. A read/write head/arm assembly consists of a read/write head assembly mounted at the end of a supporting arm structure. A track servo head/arm assembly consists of a read coil head assembly mounted at the end of a supporting arm structure.

The head assembly (Figure 3-12), which includes a cable and plug, is mounted on a gimbal ring which, in turn, is mounted on a floating arm. This method of mounting allows the head assembly to pivot (independent of the arm) tangentially and radially relative to a data track on the disk surface. Such motion is required to compensate for possible irregularities in the disk surface.

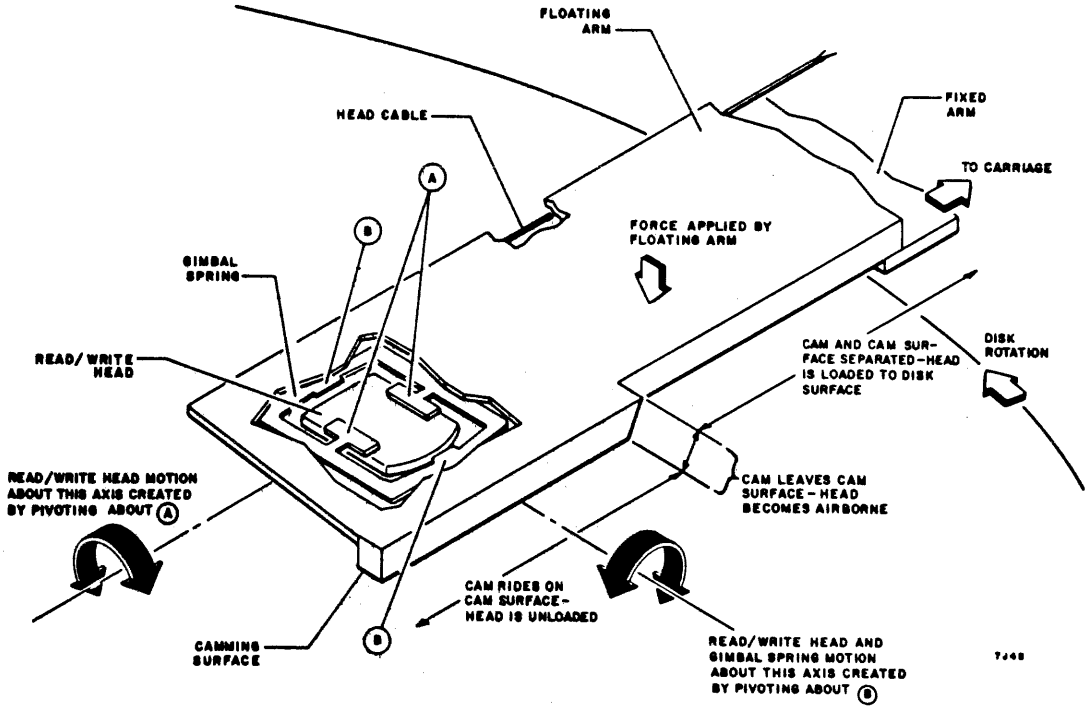


Figure 3-12. Head/Arm Assembly Motion

The arm structure consists of a floating arm secured to a heavier fixed arm. The end of the fixed arm opposite the head mounts in the carriage receiver. The floating arm is the mounting point for the head and is necessarily flexible so that it can flex during load and unload motions, onto and off of the cam surfaces.

Freedom and mobility of the head are necessary elements to being able to function with interchangeable disk packs. During head loading, each floating arm is driven off the related cam and unflexes to force a head toward the air cushion on the spinning disk surface. The force applied by the floating arm causes the heads to fly or float on the air cushion. Vertical motion by a disk surface (due to warpage or imperfection) is countered by a move in the opposite direction by the gimballed head and/or floating arm. As a result, flight height remains nearly constant.

Transducers

The deck assembly contains two transducers: speed sensing transducer and velocity transducer. These transducers provide signals that are used by the logic chassis and the controller to generally control the progression of most machine operations.

Speed Sensing Transducer

The speed sensor (Figure 3-8 and 3-12) generates a voltage output whenever a ferrous material enters the magnetic field surrounding the pole piece at the pickup end of the transducer. The spindle shaft is notched. The speed sensor generates a signal each time the notch passes the transducer. The logic then shapes this signal into a 55 μsec pulse. As long as the speed exceeds 3000 rpm, one of these pulses will be sensed at least once each 20 ms. A sensing circuit within the logic monitors the pulse repetition rate and provides an enable to Speed relay K2.

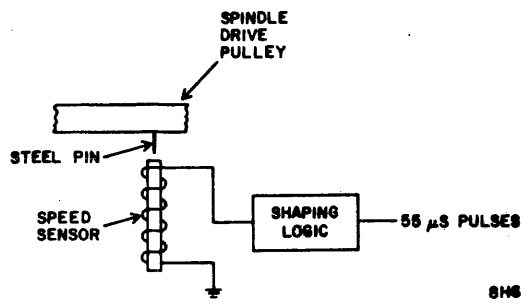


Figure 3-13. Speed Detection

If speed is insufficient, the pulse repetition rate is reduced accordingly. This has either of two effects:

1. If the heads are not loaded, K2 cannot energize and the logic will not initiate the load sequence.
2. If the heads are already loaded, K2 opens, thereby opening the coil of Retract relay K5. The voice coil is disconnected from the logic power amplifier and connected to the -16v emergency retract capacitor. The heads immediately are unloaded to the retracted stop.

Velocity Transducer

The velocity transducer (Figure 3-14) is a two-piece device consisting of a stationary tubular coil/housing and a movable magnetic core.

The magnetic core is connected via the extension rod to the rear surface of the head/arm receiver. All motion of the carriage is therefore duplicated by the magnetic core. As the core moves, an emf is induced in the coil. The amplitude of this emf is directly related to the velocity of the core (and carriage). The polarity of the emf is an indication of the direction of movement by the core (and carriage). The transducer output drives an operational amplifier located in the logic chassis. This signal is used by the servo logic to control acceleration/deceleration of the carriage during Seek operations.

First Seek Interlock Assembly S/C 09 With PE35634C & Above

The First Seek interlock assembly delays head loading for 15 seconds on a Power On/First Seek sequence. During this delay, the pack speed is stabilized and air movement in the pack purges the pack of any dust of foreign material.

The assembly consists of a motor, reset switch, cam, and a mounting base. The base mounts on the deck assembly. The motor is energized during the Power On sequence and starts a 15-second (approximate), First Seek Interlock delay cycle. The cam revolves until the reset switch is encountered.

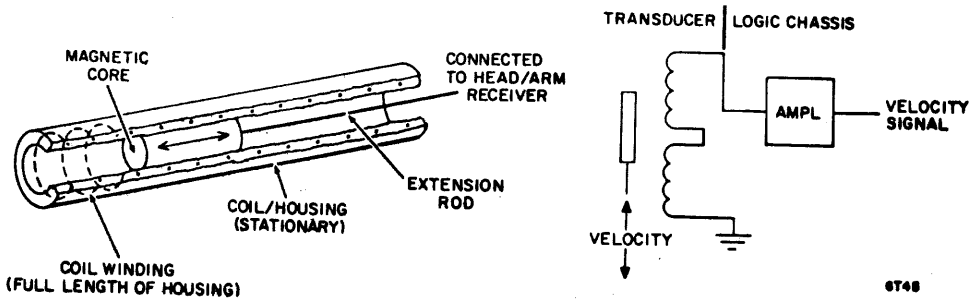


Figure 3-14. Velocity Detection

The switch then transfers and removes power to the motor and signals completion of the First Seek Interlock cycle to the logic.

If power is lost or dropped during the cycle, the cam completes the initial cycle upon reapplication of power. At this time a new cycle is initiated if speed relay K2 has not been energized. Refer to Power On paragraph for a complete description of conditions that apply power to the assembly motor.

Disk Cleaner Assembly
S/C 09 Without PE35634C & Below

The disk cleaner assembly sweeps the disk pack recording surfaces free of any foreign materials. The sweep cycle occurs before the read/write heads are loaded during the Power On/First Seek sequence.

The assembly consists of a motor, 11 comb-mounted brushes, reset switch, comb cam linkage, and a mounting base. The base mounts on the deck assembly and the brushes are pivot mounted on the base. Pivoting of the brushes is controlled by the motor, the linkage, and the switch. The motor is energized during the Power On sequence and starts a 15-second (approximate) cycle. The cam is designed so that the brushes swing in and out of the disk area during the first five seconds of the cycle. The cam then continues revolving until the reset switch is encounted. The switch then transfers and removes power to the motor and signals completion of the brush cycle to the logic.

If power is lost or dropped during the brush cycle, the operator can manually rotate the brushes clear of the disk pack so that the disk pack can be removed from the spindle. The cam then completes the initial cycle upon reapplication of power. At this time, a new cycle is initiated if Speed relay K2 has not been energized. Refer to Power On paragraph for a complete description of conditions that apply power to the brush motor.

BLOWER SYSTEM

The blower system (Figure 3-15) provides positive pressure in the pack area. The presence of this elevated pressure results in an outward dispersion of air preventing ingestion of contaminated air. This air flow greatly reduces possible contamination and resulting damage to the disk surfaces and the read/write heads.

Power to the blower drive motor is available whenever the UNIT POWER circuit breaker is on.

DISK PACK

The disk pack is the recording medium for the drive. The disk pack consists of 12 14-inch disks, center-mounted on a hub. The recording surface of each disk is coated with a layer of magnetic iron oxide and related binders and adhesives. The top and bottom disks are protective non-recording disks.

There are 19 recording surfaces and one track servo surface. The servo disk contains pre-recorded information that is used by the servo logic to position the heads to the desired track.

The 411 recording tracks are grouped in a 2-inch band near the outer edge of the disk. Track 411 has a diameter of approximately 9 inches, while the diameter of track 0 is about 13 inches. The tracks are spaced about 0.005-inch apart.

The disk pack has a two-piece container. The bottom

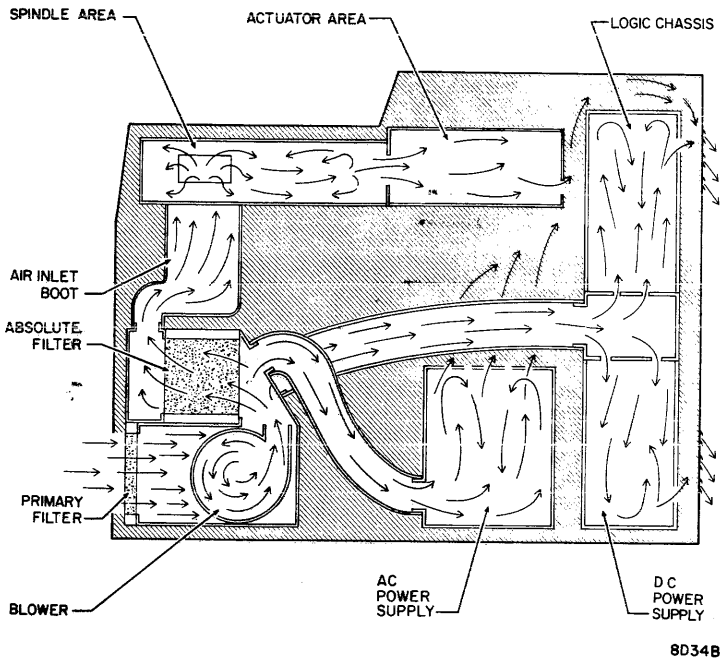


Figure 3-15. Blower System

cover can be removed simply by grasping and rotating the center hub. The top cover is designed so that it can be removed only by installing the disk pack on the spindle. The disk pack can be removed from the spindle only by using the top cover (see Operation section). This design protects the disk pack from physical damage and greatly reduces the possibility of contamination of the disk pack recording surfaces.

LOGIC FUNCTIONS

The logic functions performed by the drive are subdivided as follows:

- Basic Interface Description
- Unit Selection
- Seek Operations
- Basic Read/Write Principles
- Write Operations
- Read Operations

Most operations require the transfer of data between the controller and the drive. Descriptions of these signal interchanges will emphasize drive functions. Controller functions are described only where necessary to clarify drive operations. Unless otherwise specified, controller signal timing is for illustrative purposes only. Refer to the applicable controller manual for details of controller operations and actual I/O timing.

BASIC INTERFACE DESCRIPTION

Signals are exchanged between the controller and drive by means of two signal cables. These cables are the "A" (Address/Control) cable and the "B" (Data) cable. Dual-channel units have a pair of cables for each controller.

Data is transmitted between the controller and drive by two sets of data bus lines. These lines are numbered from bit 0 (2^0) through bit 8 (2^8). The significance of the data on these lines is indicated by one of 14 tag (control) lines manipulated by the controller. Five of these tag lines cause the drive to accept input information from the controller while the other nine tag lines cause the drive to supply data to the controller. Additional lines transfer selection, powering, and status information without regard to the tag lines.

Figure 3-16 is a block diagram of the drive and its I/O lines. The encircled numbers assist in determining the relationship between the tags and the

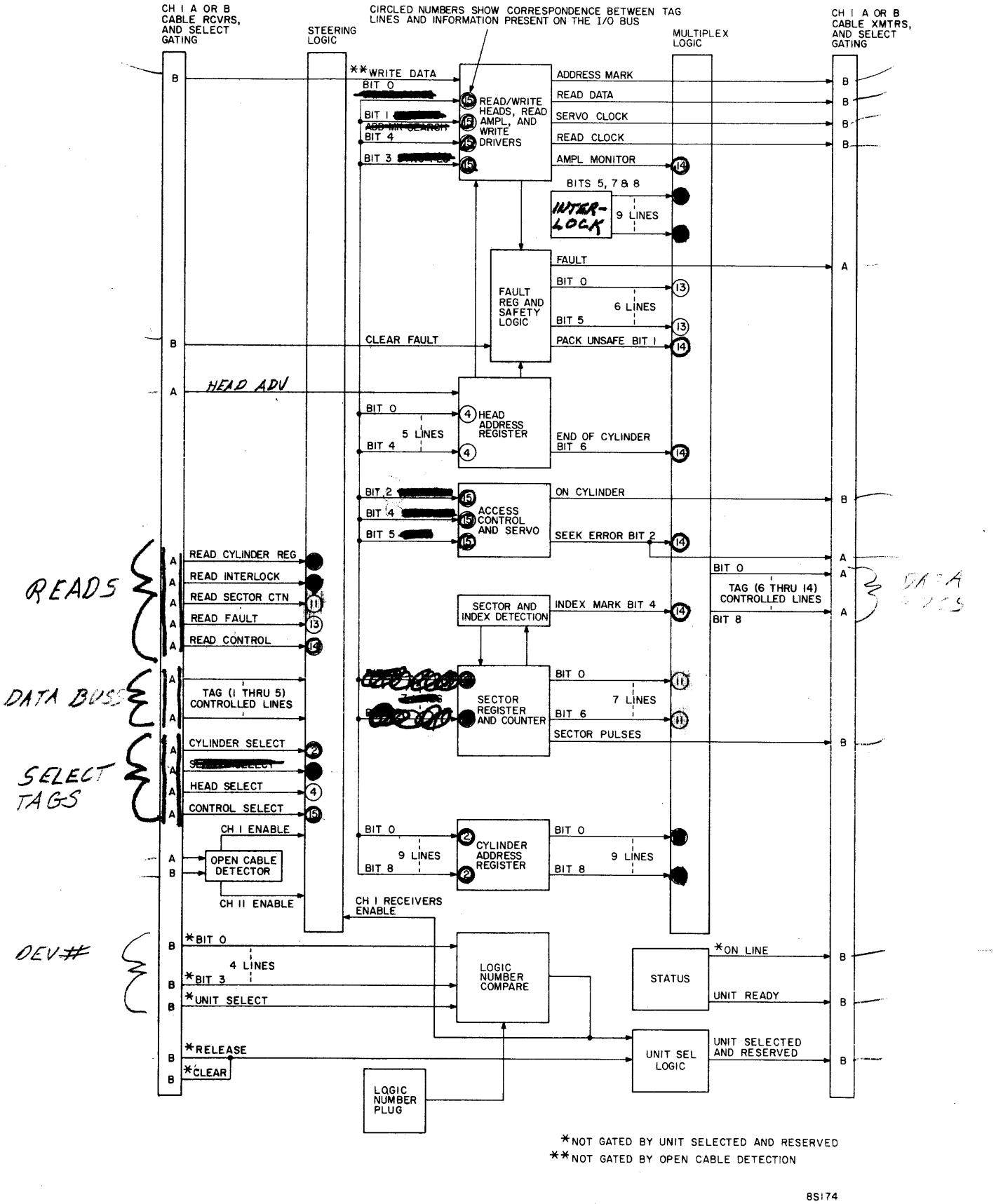


Figure 3-16. DSU Block Diagram, Dual or Single Channel

information on the bus lines. For example, note that the Head Address register block shows bits 0 through 4 as an input with a circled "4" within the block. This indicates that these five bits are gated into the register when the Head Select tag is up.

The block diagram shows only the main elements involved in the I/O dialog. More detailed diagrams that illustrate signal interchanges between drive logic subsystems are provided in the applicable theory portion of this manual.

Definitions of the signals on the I/O lines are provided by Table 3-1. Table 3-2 defines the meanings of the bits on the bus lines in accordance to the active tag.

TABLE 3-1. I/O LINES

Source	Signal Name	Function
		"A" Cable Lines
Drive	Output Bus Lines	Nine lines that supply data to the controller as directed by the active tag line.
Controller	Input Bus Lines	Nine lines that supply data to the drive. Meaning of the data is a function of the active tag line.
Drive	Seek Error	Status line indicating that one or more of the following errors occurred: 1. Drive could not complete seek (including RTZS) within 500 ms following receipt of seek command. 2. Drive went Off Cylinder for more than 800 μsec during non-seek condition. 3. Heads went forward past cylinder 410 (Forward End of Travel) or went reverse past cylinder 000 (Reverse End of Travel). Not applicable while performing on RTZS. Signal is returned only to selected channel. NOTE Remaining "A" Cable signals are tag lines. Refer to Table 3-2 for bit significance of information on data lines during these tags
Controller	Cylinder Select	Tag line indicating that input bus lines contain new cylinder address to be loaded into Cylinder Address register.
Controller	Head Select	Tag line indicating that bus data lines contain head number to be entered into Head register. Head cannot actually be selected for 6 μsec after receipt of command or if Off Cylinder.
Controller	Read Cylinder Status	Tag line commanding drive to place current cylinder address from Cylinder Address register onto ~~input~~ output bus lines.
Controller	Read Fault Status	Tag line commanding drive to gate contents of Fault register onto output bus lines.
Controller	Read Control Status	Tag line commanding drive to gate selected control functions onto output bus lines.

TABLE 3-1. I/O LINES (Cont'd)

Source	Signal Name	Function
Controller	Head Advance	This signal advances the head counter by one. Head advance occurring with end of cylinder, clears the head counter.
Drive	Fault	Sent to the controller when the Fault FF is set.
		"B" Cable Lines
Drive	Unit Ready	Status line indicating that heads are loaded (First Seek completed). Unit will not accept Seek, Read, Write, or Release commands unless this line is true. Signal drops when heads unload.
Drive	On Line	Ground indicates that mode switch on maintenance panel is ON LINE position. Open circuit indicates that switch is in OFF LINE or WRITE DISABLE.
Drive	Read Data	The Read Data signal is the phase lock compensated signal read directly from the disk.
Controller	Write Data	Write Data is the serial MFM coded signal that is sent over the I/O from the controller to the DSU to be recorded on the disk.
Controller	Clear Fault	Clears Fault FF (thereby extinguishing FAULT indicator) and Fault register. Contents of Fault register are gated onto output bus lines by Read Fault Status tag.
Controller	Logic Number Lines (4)	Used during drive selection these lines contain the logical address of the drive to be selected. If the contents of these lines match the drive address (as indicated by the logic plug), the drive will raise its unit selected line indicating it is selected.
Controller	Unit Select	Initiates drive selection and is used in conjunction with the logic number lines.
Drive	Unit Selected	Indicates that drive is On Line and has accepted a Unit Select command. Unit Number indicator on control panel lights.
Drive thru Controller	Power Sequence Lines (6)	Used to sequentially power up drives under controller control. Refer to Power Supplies theory for information.
Drive	Address Mark	Indicates the address mark gap or an inter-record gap. It is initiated by the PLO being in a fast start condition.
Drive	On Cylinder	Indicates unit has completed a move to the addressed cylinder.
Drive	Read Clock	Clock signal recovered from raw MFM data by the data separator. It defines the beginning of a data cell.

TABLE 3-2. TAG LINES/DATA LINES

Tag Line	Data Line Bit	Name/Meaning
	Refer to Table 3-1 for tag line functions.	
Cylinder Select and Read Cylinder Register	0	1
	1	2
	2	4
	3	8
	4	16
	5	32
	6	64
	7	128
	8	256
Control Select	0	Write Gate. Enables write driver. Not accepted if there is Seek Error or Fault status.
	1	Read Gate. Enables read logic to recognize read data on pack and to place digital data on Read Data Lines.
	2	Forward Offset. If the difference counter equals zero, a 400 (±40) μin forward carriage offset results. Carriage position returns to nominal when the signal goes false. Movement of the carriage does not result in loss of On Cylinder status. NOTE Forward Offset, Reverse Offset, Data Strobe Early, and Data Strobe Late are intended to aid marginal data recovery.
	3	Sync PLO. Causes phase lock oscillator to sync on zeros in gap areas with no Address Mark. This syncs read circuitry to data being read.
	4	Address Mark Search. Indicates Address Mark (24 bits of missing data) and data preamble (to record one or greater) are being searched. During a write mode, this signal is raised to inhibit the write fault circuits while no write driver transitions are occurring.
	5	Reverse Offset. If the difference counter equals zero, a 400 (±40) μin reverse carriage offset results. Carriage position returns to nominal when the signal goes false. Movement of the carriage does not result in loss of On Cylinder status.

TABLE 3-2. TAG LINES/DATA LINES (Cont'd)

Tag Line	Data Line Bit	Name/Meaning
Control Select (Cont'd)	6	Return to Zero. Causes drive to perform Return to Zero Seek if Fault status is not up. The following occur: 1. Actuator returns to cylinder 000 at 7 ips. 2. Cylinder Address register set to zero. 3. Difference counter set to 511 (T=0). 4. Seek Error FF cleared if an error exists. This drops Seek Error signal to controller. 5. Will cause Read Control Status bit 2 (Seek Error) to clear. 6. Will cause Read Fault Status bit 5 (Seek Error) to clear after receipt of Clear Fault signal. (Seek Error itself does not set Fault FF.)
	7	Data Strobe Early. Causes read data strobe to be moved to the early position of the data window. (Data strobe occurs about 8 nsec earlier than normal.) Data strobe timing returns to normal when command signal goes false.
	8	Data Strobe Late. Causes read data strobe to be moved to the late position of the data window. (Data strobe occurs about 8 nsec later than normal.) Data strobe timing returns to normal when signal goes false.
Read Fault Status		NOTE All bits except 5, set the Fault FF: FAULT indicator lights: Seeks, RTZS, Reads, and Writes are not executed. A Clear Fault command is required to clear the bits.
	0	(W+R) · $\overline{\text{On Cylinder}}$. A write or read gate was received while actuator is not On Cylinder.
	1	W · R. A write was received while reading.
	2	Current. With the heads loaded, one or more of the following errors occurred: 1. More than one head is selected for greater than 7.5 μsec. 2. Both write drivers on simultaneously. 3. Write gate on but no data transitions for 900 nsec (no write data or open write coil).
	3	+Volt. +20v power less than +18v or +5v power less than +4.825v.
	4	-Volt. -20v power more positive than -18v or -5v power more positive than -4.825v. Also generated if -16v emergency retract voltage is more positive than -12v. Heads retract to unloaded position.
	5	Seek Error. Drive could not complete a normal seek. Refer to Seek Error in Table 3-1 for causes. Fault FF is not set.
	6-8	Not Used

TABLE 3-2. TAG LINES/DATA LINES (Cont'd)

Tag Line	Data Line Bit	Name/Meaning
Read Control Status	0	Not Used.
	1	Pack Unsafe. Fault FF is set. FAULT indicator is on. One or more of the following occurred: 1. (W+R) · On Cylinder fault. See bit 0 of Read Fault status. 2. W · R fault. See bit 1 of Cylinder fault. 3. Current fault. See bit 2 of Read Fault status. 4. Voltage fault. See bit 3 and 4 of Read Fault status.
	2	Seek Error. Drive could not complete a normal seek. Refer to Seek Error in Table 3-1 for causes.
	3	
	4	Index. A track reference pulse that occurs once per revolution.
	5	Not Used.
	6	~~End of Cylinder. Head Advance signal (bit 3 of Control Select) or Head Select tag has caused Head register to contain decimal 19 or greater.~~
	7-8	Not Used.

was removed for O.G.

The drive must be selected before it can accept any commands from the controller. Selection is accomplished by means of the Unit Select Log.

The drive is selected when the Unit Select line goes true and Logical Number bits 0-3 match the drive address. The drive address is determined by the drive's Logical Number plug. When selection is complete the drive raises its Unit Selected and Reserved line. The line remains true and the drive remains Selected until the controller drops one Unit Select line or changes the contents of the Logical Number bits.

SEEK OPERATIONS

Seek operations are those drive functions that cause a repositioning of the read/write heads. The heads are attached to the actuator which, in turn, is moved by a voice coil positioner. The mechanical elements involved in the mechanism are described in the assembly portion of this section.

Two logic circuits are used to control the seek functions:

1. The Servo Circuit, which controls the voice coil positioner.
2. The Track Servo Circuit, which generates signals relating to the position of the heads over the disk pack.

NOT USED

The general concepts of these two circuits are explained to provide the general background information needed to understand the specific types of seeks. Then more detailed explanations are provided for the three types of seeks: First Seek, Direct Seek, and Return to Zero Seek.

SERVO CIRCUIT

The servo circuit is a closed loop servomechanism used to position the read/write heads. Figure 3-18 is a simplified schematic of the servo circuit. Functions of the major elements of the system are explained in Table 3-3.

TABLE 3-3. SERVO CIRCUIT FUNCTIONS

Circuit Element	Function
Difference Counter	Holds the complement of the number of tracks yet to be crossed before reaching the desired track or cylinder. Counter value is decimal 511 when on cylinder. An associated decoding network provides outputs representative of the current general content of the counter.
Digital to Analog Converter	Monitors the five lowest order bits of difference counter to provide an analog indication of Position Error during the last 32 tracks (except last track) of all Seek operations.
Position Converter	Provides coarse Position Error signal, the amplitude of which is proportional to the number of tracks to go. Amplitude is clamped at negative saturation while tracks remaining are equal to, or greater than 32. Amplitude decreases in discrete steps (controlled by D/A converter) as last 32 tracks of a seek are crossed. Signal is inverted for reverse seeks.
Desired Velocity Function Generator	Processes Position Error signal at gain levels that vary as Position Error decreases. The resulting output is the analog representation of the desired velocity curve to achieve maximum control of deceleration. When tracks remaining become less than 64, a low resistance (9.09K) negative feedback path is enabled that decreases generator gain. The parallel non-linear feedback circuit maintains tight loop control by increasing gain as the Position Error signal approaches zero. This gain control prevents loss of control during the critical deceleration portion of the seek and is essential to minimize overshoot and settle out problems. It also minimizes drift about null.
Summing Amplifier	Generates a control signal to drive the power amplifier. Control signal based on algebraic summation of Position Error and Velocity Amplifier signal causes power amplifier to accelerate carriage. When Velocity signal exceeds Position Error, carriage decelerates.
Load Gate	Provides a constant positive input to the summing amplifier. This causes forward velocity of 7 ips.
RTZ Gate	Provides a constant negative input to the summing amplifier. This causes reverse velocity of 7 ips.

TABLE 3-3. SERVO CIRCUIT FUNCTIONS (Cont'd)

Circuit Element	Function
Power Amplifier	Responds to summing amplifier derived control signal to drive carriage mounted voice coil positioner. Current feedback is used to stabilize the gain of the power amplifier.
Velocity Amplifier	Amplifies signal of carriage mounted linear velocity transducer to provide an indication of velocity to the servo circuit. Also receives a negative feedback from positioner which acts to cancel current coupling that occurs from the velocity transducer location within the magnetic field created when current is applied to the voice coil positioner. The associated amplifier disable forces amplifier gain to zero during a Power Off sequence (unload heads). This is required so that coupling between the positioner field and the velocity transducer does not cause oscillation during movement to the retracted position.
Velocity Integrator	Provides an integrated representation of velocity between each of the last 32 track pulses of a seek. Integrator is clamped off to gain of zero at all other times. Integrator output is a sawtooth waveform applied to input of desired velocity function generator between each track pulse to fill in or smooth out the stepped signal of the D/A converter (received via the position converter).
Fine Enable and Fine Latch	Fine enable monitors integrated velocity. When difference counter is 510 (T=1) and fine enable (Velocity integrator output) exceeds 1.28v, it indicates that there is one-half track to go. Fine latch sets to enable fine gate and disable coarse gate. This switches Position Error input to summing amplifier from desired velocity (coarse gate) to fine servo (fine gate). Fine also has the following effects: a. Turns on integrator clamp to switch off velocity integrator. b. Enables on cylinder detection. During load or RTZ sequences, both outputs of Fine latch are high. This disables both the fine and coarse gates so that motion is under control of load gate or RTZ gate.
Bit 0 Address Register and Slope FF	Used to select proper track servo signal phase for use as Fine Servo signal (signal controlling servo loop as last track is approached and carriage is stopped). If bit 0 is not set, the seek destination is an even numbered track, the Slope FF clears at Start Seek pulse, and the track servo signal will be inverted for use in stopping the carriage. If bit 0 is set, an odd track is identified, and Slope FF sets at Start Seek pulse, and track servo is not inverted.
Fine Position Amplifier	Provides the Fine Position signal to the On Cylinder Detector and to the fine servo amplifier. This signal amplitude is proportional to distance that heads are displaced from track centerline. Scale factor is one volt per 0.001-inch displacement.

TABLE 3-3. SERVO CIRCUIT FUNCTIONS (Cont'd)

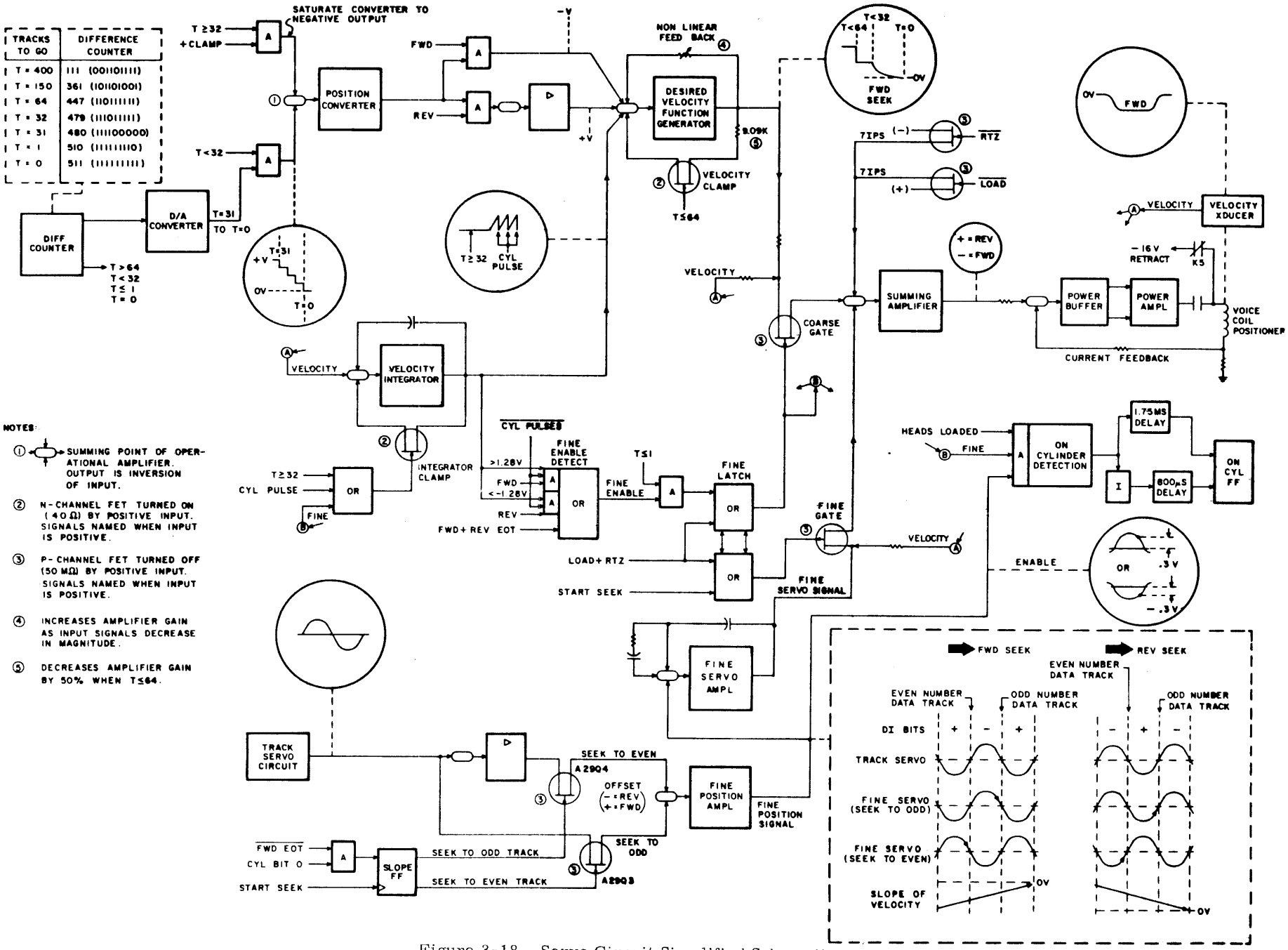
Circuit Element	Function
Fine Position Amplifier (Cont'd)	If heads drift off slightly after seek is completed, track servo signal is no longer null. This becomes fine position signal to drive heads back into position. Carriage may be offset 400 microinches from nominal track centerline by application of offset voltage to fine position amplifier. This voltage may be applied either by controller or by drive maintenance panel.
Fine Servo Amplifier	Provides the Position Error signal, via the fine gate, to the summing amplifier during the last one-half track of the seek. Amplitude of this signal is proportional to distance-to-go. Because this amplifier is connected as a differentiating amplifier, loop gain is slightly greater when switching into fine mode. (This effect is result of ac component inherent to positioner motion.) As positioner settles in at cylinder 000, differentiation effect becomes negligible and amplifier functions as inverting amplifier with dc gain of one. Phase is selected by Slope FF to be opposite in phase to velocity signal. The combination of the position error and velocity signals controls voice coil current to bring positioner into On Cylinder position.
On Cylinder Detector	Monitors fine position signal when $T \leq 1$. When signal is less than about 0.3v, heads are close enough to track centerline to be assumed to be on cylinder. After 1.75 ms delay, On Cylinder is generated. If heads overshoot at end of seek so that voltage exceeds 0.7 volt, delay is re-initiated. Delay permits carriage to settle out before controller may attempt any read/write operations.

A servo loop sums all of the error voltages imposed on it. The loop always attempts to maintain itself at a null. If not nulled, the loop will adjust the correctable device (in this case, the voice coil positioner) to achieve this null. Signals applied to the loop are called error voltages. Two major error voltages are used:

1. A position error: this is the departure of the positioner from the desired position.
2. A feedback signal to modify (or oppose) the position error to cause a smooth motion of the positioner.

The position error signal is provided by the position converter and its allied elements. The amplitude of the signal is proportional to the distance from the present position to the desired position (tracks-to-go). The major feedback signal is the output of the velocity transducer. The amplitude of this signal is proportional to the velocity of the positioner while the phase indicates the direction of motion, forward or reverse.

The loop applies its position and feedback signals to one summing point, the summing amplifier. If the summation of these signals is not equal to zero, the



NOTES:

① SUMMING POINT OF OPERATIONAL AMPLIFIER. OUTPUT IS INVERSION OF INPUT.

② N-CHANNEL FET TURNED ON (40 Ω) BY POSITIVE INPUT. SIGNALS NAMED WHEN INPUT IS POSITIVE.

③ P-CHANNEL FET TURNED OFF (50 MΩ) BY POSITIVE INPUT. SIGNALS NAMED WHEN INPUT IS POSITIVE.

④ INCREASES AMPLIFIER GAIN AS INPUT SIGNALS DECREASE IN MAGNITUDE.

⑤ DECREASES AMPLIFIER GAIN BY 50% WHEN T≤64.

Figure 3-18. Servo Circuit Simplified Schematic

150 M BYTE #3-8 5

summing amplifier outputs a signal proportional to the amplitude of the error voltage (which signifies the amount of displacement from the desired position) and the phase of the error voltage (which indicates the direction of displacement).

The error output from the summing amplifier is applied to the actuator assembly. The actuator contains a voice coil positioner that supports and moves the read/write heads. In turn, the voice coil is located within a powerful magnet. Whenever a current passes through the voice coil windings, the interaction of the induced emf and the magnet's flux field cause the positioner to move. The acceleration of the motion is proportional to the polarity and amplitude of the voice coil current.

Basic Seek Operation

Seek operations are initiated by a series of control signals from the controller or by internally-generated signals within the drive during power up conditions. Most long seeks may be divided into four phases (see Figure 3-19):

1. Accelerate Phase: the voice coil receives full current to move the positioner from the current cylinder towards the new cylinder.
2. Coast Phase: velocity is at its maximum and the positioner velocity is constant.
3. Deceleration Phase: the positioner is approaching the desired cylinder. Its velocity must be reduced by braking action to prevent overshoot.
4. Stop Phase: the positioner is almost at the desired cylinder. It must be stopped at the precise centerline of the new data cylinder. The logic is in Fine mode to stop and hold the positioner at the new cylinder.

Refer to the various seek descriptions for detailed information on the exact seek sequencing.

Accelerate Phase

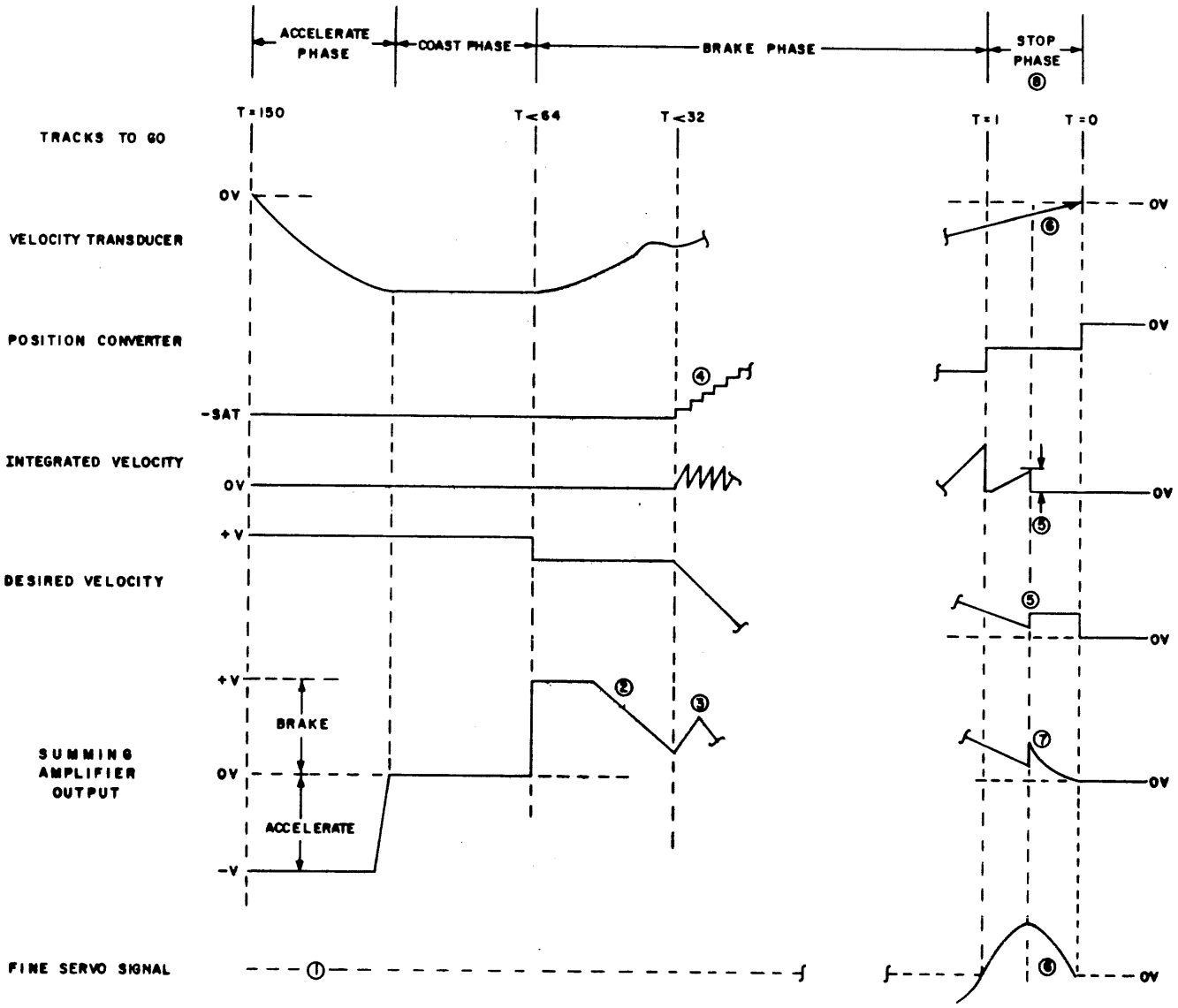
This phase is controlled largely by the position error signal. The controller sends the desired cylinder to the unit. The new address is complimented and added to the old address. The New Address Generator performs this addition and generates a difference. The compliment of the difference is loaded into the Difference Counter. For example, if the heads are presently on cylinder 10 and must go to cylinder 160, the seek length is 150 cylinders. In binary representation, decimal 150 is 0 1001 0110. The complement of this number is 1 0110 1001, or decimal 361. At each cylinder pulse, the counter is incremented; therefore, the greater the number in the difference counter, the fewer tracks-to-go. The counter is at its maximum value of 511 (1 1111 1111) when tracks-to-go equals zero.

The five low-order bits of the difference counter are applied to the position converter. The value of these bits indicates the position error (or tracks-to-go) from 0 to 31. That is, the amplitude of the position converter output is directly proportional to the number of tracks remaining in the seek. If the remaining seek length is greater than 31 ($T \geq 32$), the position converter output is clamped at its maximum saturated value to cause a very large position error.

The input to the summing amplifier is now a large signal. Since there is no velocity yet, the current through the voice coil is maximum, causing maximum acceleration. As the positioner accelerates, a velocity signal is generated by the velocity transducer. This signal opposes the position error signal. Its amplitude, however, is less. Acceleration continues.

Coast Phase

Eventually, the amplitude of the position error signal and the velocity feedback signal are equal. The net error signal in the loop drops to zero. The summing amplifier output follows, so current is cut off. Velocity is constant. Friction losses will tend to slow the positioner but, as it does, the velocity signal decreases. This allows the position error signal to call for more current.



NOTES:

① SIGNAL HAS NO EFFECT UNTIL FINE LATCH SETS.

② SLOPE DETERMINED BY LOOP GAINS TO PERMIT SERVO CONTROL ALONG DESIRED CURVE.

③ GAIN CHANGE CAUSED BY ADDITION OF INTEGRATED VELOCITY SIGNAL TO POSITION CONVERTER SIGNAL.

④ OUTPUT DECREASES WITH EACH CYLINDER PULSE.

⑤ FINE LATCH SETS WHEN $T \leq 1$ AND INTEGRATED VELOCITY $> 1.28V$. DESIRED VELOCITY HAS NO FURTHER EFFECT.

⑥ COMBINATION OF THESE TWO SIGNALS CONTROLS OUTPUT FROM SUMMING AMPLIFIER.

⑦ GAIN CHANGE CAUSED BY SWITCH FROM COARSE TO FINE CONTROL. ALTHOUGH CONTINUOUS BRAKING ACTION IS ILLUSTRATED, OUTPUT MAY BE NEGATIVE (ACCELERATE) IF FINE SERVO SIGNAL EXCEEDS VELOCITY SIGNAL.

⑧ SCALE CHANGED AT T=1 FOR CLARITY.

9. DRAWING NOT TO SCALE FOR TIMING OR RELATIVE SIGNAL AMPLITUDE. IT IS SIMPLIFIED TO ILLUSTRATE SIGNAL FUNCTIONS.

7J120A

Figure 3-19. Servo Circuit Simplified Signals

Decelerate Phase

Braking action starts as the positioner approaches its selected cylinder.

The track servo circuit (refer to Track Servo Circuit description) has been generating cylinder pulses as each cylinder is passed. These pulses are used to increment the difference counter. When T=64, the position error signal from the desired velocity function generator is reduced. This causes the velocity signal to dominate and, since it is opposite in phase to the position error, the summing amplifier output switches polarity. Opposing current passes through the voice coil. The carriage decelerates.

Deceleration continues until the velocity and position signals are again equal. This occurs when velocity is about one-half of its maximum value. A secondary Coast Phase is entered until T < 32.

When T < 32, another Decelerate Phase begins. The loop maintains speed along an ideal velocity curve. This curve is the analog version of the number of tracks-to-go. The velocity curve is generated by the desired velocity function generator. Its output is compared with velocity to achieve maximum deceleration under all conditions without overshoot. The deceleration curve permitting the best control is obtained by taking the square root of the position signal and comparing it with velocity. The position signal is the sum of the following:

1. The position error signal from the position converter. Its output, which is now unclamped, is a signal whose amplitude is proportional to the number of tracks-to-go.

2. Integrated velocity from the velocity integrator. Integrating a velocity signal provides a signal proportional to distance. This signal is a sawtooth waveform: it is pulled back to zero by each cylinder pulse and increases in proportion to velocity and time (distance). The combination of the stepping-down output from the position converter with the ramp integrated velocity signal results in a smooth curve of constantly-decreasing magnitude.

3. The square root function provided by the non-linear feedback around the desired velocity function generator.

Both the desired velocity and velocity signals are decreasing simultaneously. Current (which is still braking) decreases proportionately. The system servoes about the ideal curve; velocity and braking current are both decreasing.

Stop Phase

Stop Phase begins when the difference counter indicates that there is one track-to-go. When T=1, the velocity integrator signal is pulled back to zero by the cylinder pulse. Its output, indicating distance, increases. When its amplitude indicates approximately one-half track remains, Fine Enable sets the Fine latch. Desired velocity is disabled since the coarse gate is opened by Fine being set.

The last half-track of motion is controlled by the fine servo signal. There is a slight increase in position error gain in switching from coarse to fine. Fine servo and velocity are applied to the summing amplifier through the fine gate. The summation of these two signals control the braking current.

At the start of the seek, the Slope FF is set if the seek is to an odd-numbered cylinder. The odd cylinder signal controls the phase of the track servo signal applied to the fine position amplifier. This adjustment is required since track servo signal phasing is a function of the servo head position: the signal is positive when over negative dibits and negative when over positive dibits. Therefore, on forward seeks, the signal is decreasing from a positive value toward zero when approaching a data track with an odd number; it is increasing from a negative value toward zero when approaching a data track with an even number. The opposite is true during a reverse seek.

Phasing of the track servo signal is selected so that the fine servo signal opposes the velocity signal during the last half-track of the seek. Both signals are decreasing. If either is greater, the summing amplifier makes minor braking current adjustments. When the heads are on cylinder, both signals are zero and current is zero.

When the fine position signal (equal in amplitude, but 180 degrees out-of-phase with the fine servo signal) is less than about 0.3v, the positioner is, for all practical purposes, positioned over the data track. This initiates the On Cylinder delay. After 1.75 ms, On Cylinder is generated.

The fine servo and fine position signals remain active even though On Cylinder is up. This is the track following or position error operation. Since the positioner is not mechanically locked in place, it can drift off cylinder. As long as it is precisely positioned, the dibits read from the adjacent dibit tracks are equal and opposite. Should the carriage move, one dibit signal will increase in amplitude. This results in a slight track servo signal which is translated into the fine servo signal. The summing amplifier, in turn, senses this off-null condition and drives the positioner back on cylinder.

If the positioner goes off cylinder sufficiently to cause the fine position signal greater than 0.7v for more than 800 μsec, the On Cylinder signal is lost. This sets Seek Error, and deselects the heads. If the unit is reading or writing at the time Fault is also set.

The loop also permits positioner offset if the program requires it for error recovery. A Forward Offset command (Control Select and bit 2) with a zero-length seek indicated by the difference counter will provide a positive bias input to the fine position amplifier. This is now an error signal to the summing amplifier to cause a motion forward of 400 microinches. The motion stops when the bias voltage and track servo voltage cancel. Reverse Offset (Control Select and bit 5) with a zero-length seek indicated by the difference counter causes a 400-microinch reverse offset. Either offset may also be provided by switches on the maintenance panel.

Short Seeks

The preceding explanation of the basic seek operation presumed long seeks that permitted the positioner to attain maximum velocity. Maximum velocity of about 65 ips requires 70 tracks acceleration time. During short seeks, gating is identical although relative phasing of the error signals will vary.

During seeks less than 32 tracks, certain signals are available immediately: integrated velocity, nonlinear feedback to the desired velocity function generator, and a position converter output not clamped at its maximum value. These signals generate a position error voltage to accelerate the positioner. Because the amplitude of the desired velocity signal is less, however, the voice coil current is not as great as during long seeks.

The net effect of these differences is that system gain is reduced. Acceleration is reduced accordingly to permit minimum total seek time while not permitting over-acceleration that would cause overshoot. The primary function remains unchanged: acceleration occurs when the position error signal exceeds the velocity signal; braking occurs when the velocity signal exceeds the position error signal.

TRACK SERVO CIRCUIT

Basic Description

The track servo circuit provides head positioning information. The signals generated by this circuit:

1. Generate a track servo signal that indicates the displacement of the heads from their nominal track centerline.

2. Generate indications that the heads are positioned outside of the normal data cylinders.

3. Generate cylinder pulses during seeks to indicate each cylinder crossing.

4. Provides signals used as the basic 806 kHz clock.

Information for this circuit is derived from the track servo head (Figure 3-20). This head is physically similar to the read/write heads, except that it does not write. The head reads information from the servo track surface of the disk pack. This information is known as dibits; dibit is a shortened term for dipole bit. Dibits are prerecorded on the servo surface during manufacture of the disk pack. Do not confuse the servo surface with the other 19 disk pack recording surfaces.

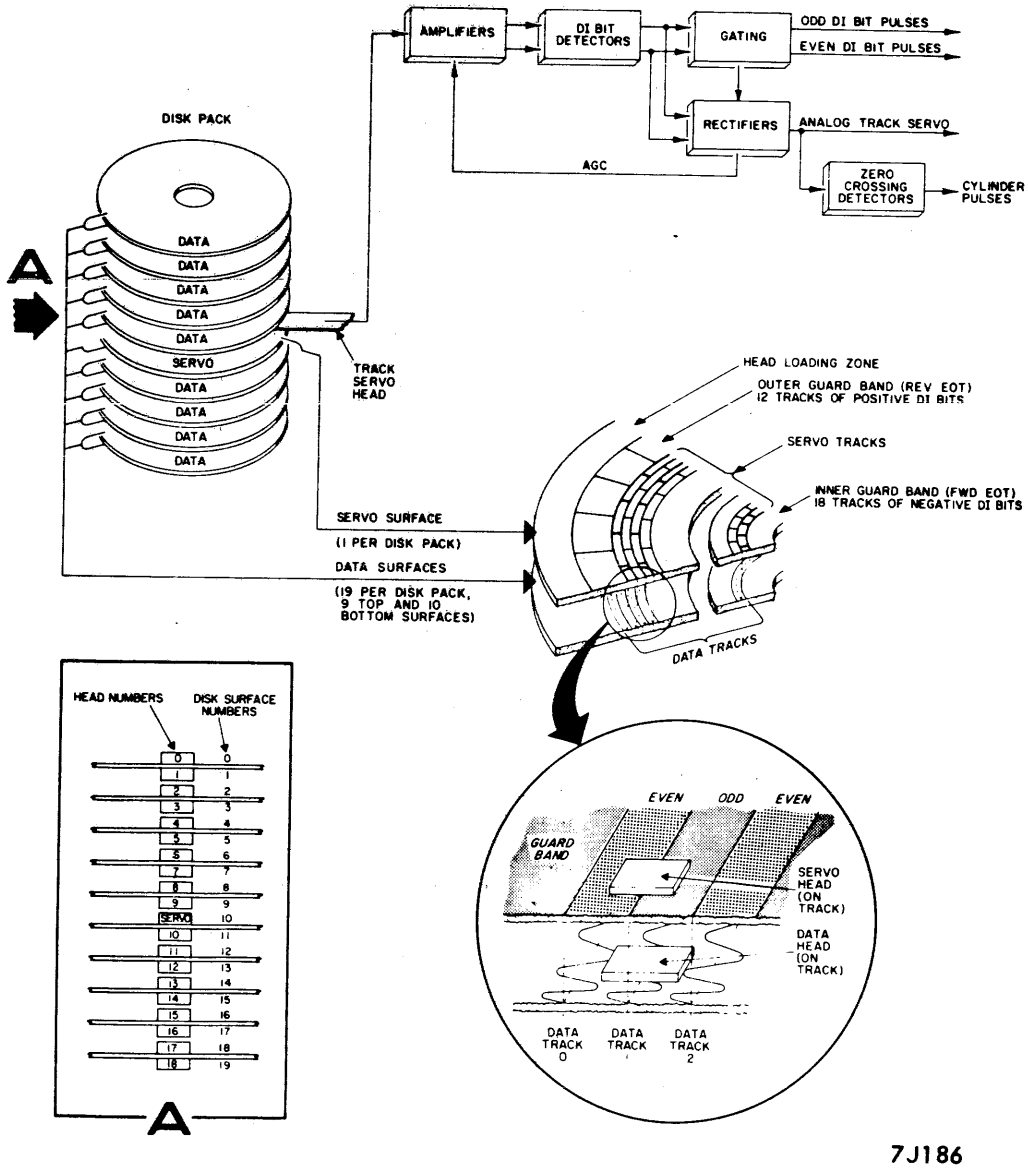


Figure 3-20. Track Servo Disk Layout

Dibits are the result of the manner in which flux reversals are recorded on the servo tracks. One type of track, known as the Even track, contains negative dibits. The other track, the Odd track, contains positive dibits.

There are 440 dibit tracks on the servo surface. At the outer edge of the surface is a band of 12 positive dibit tracks. This area is the Reverse End of Travel (EOT) or outer guard band. Then, there are 410 servo tracks alternately recorded with negative and positive dibits. Finally, toward the inner edge of the pack, there are 18 tracks containing only negative dibits. This is the Forward EOT or inner guard band.

When the read/write heads are located at the centerline of a data track, the track servo head is actually centered between two of the prerecorded servo tracks and is reading an edge of each. The detected signal is a mixture of the two adjacent dibit signals. The amplitude of each dibit component is proportional to the read coil overlap of the recorded servo tracks. With the head centered, the amplitudes of the two types of dibits are equal. As the head moves away from its centered position, the amplitude of one dibit component increases while the other decreases. This error voltage is the track servo signal.

Circuit Description

The basic elements of the track servo circuit are illustrated in Figure 3-21. Table 3-4 explains the track servo circuit functions.

Dibit Gating

After being differentially amplified, the servo signal is applied to gates that separate the dibit signals by sensing the positive and negative flux reversals (Figure 3-22). A positive dibit consists of a positive-going waveform immediately followed by a negative-going waveform. On the other hand, a negative dibit consists of a negative-going waveform followed immediately by a positive-going waveform. This component triggers the End Dibits one-shot.

The dibits are analyzed by the positive and negative gates. Each gate output switches to the low state when it senses its respective dibit. The negative-going pulses control single-shots and JK FF's to generate the odd/even dibits.

The even/odd dibits are used to enable the EOT detection circuit and to generate the basic machine clock signal.

Track Servo Signal

The servo signal is generated by peak detectors that monitor their respective dibits. The positive and negative peak detectors sample and hold the peak voltage of their respective dibit peaks. The outputs of each are gated by their respective delays. When the delay input is low the peak detector is inhibited, when it is a logic one the output is a function of the amplitude of the dibit signal. The capacitor used to store the peak voltage is connected to the inverting input of the peak detector. The peak detector buffers buffer the peak holding capacitors and invert the polarity for proper input into the agc amplifier.

The track servo signal is provided by an operational amplifier connected as a differential amplifier. The differential amplifier monitors the peak detector buffers and outputs a voltage directly proportional to the difference between the peak amplitudes of the odd and even dibits.

The track servo signal is at its maximum negative value when the servo head is positioned over the outer guard band or over one of the odd dibit tracks. It is at its maximum positive value when the servo head is positioned over the inner guard band or over one of the even dibit tracks.

The track servo signal is applied to the servo circuit and to the cylinder detect circuit. In the servo circuit, it is used to generate the fine servo signal that controls movement during the last one-half track of a seek or during a Load sequence. The cylinder detect circuit generates cylinder pulses as the track servo signal approaches a null.

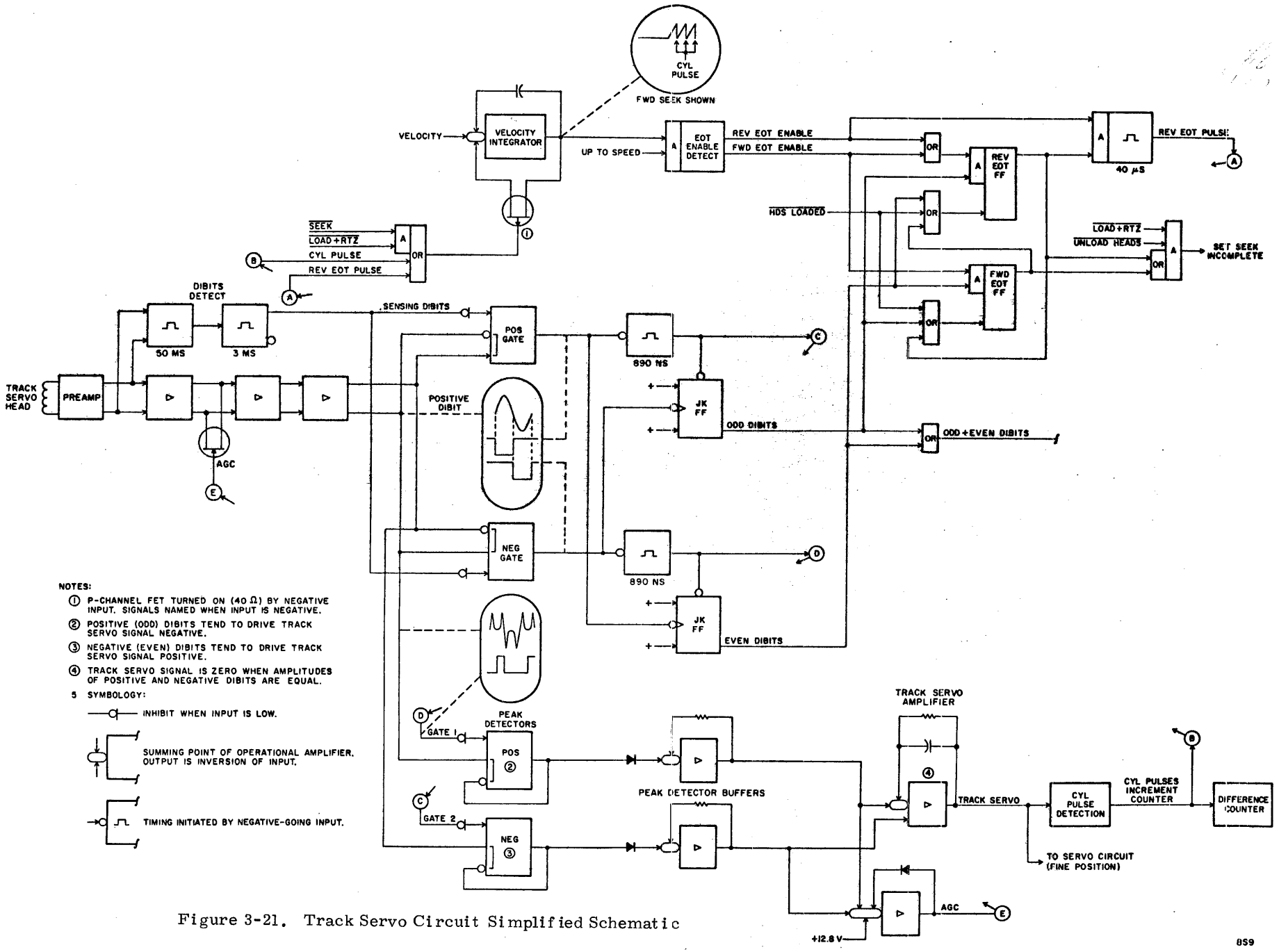


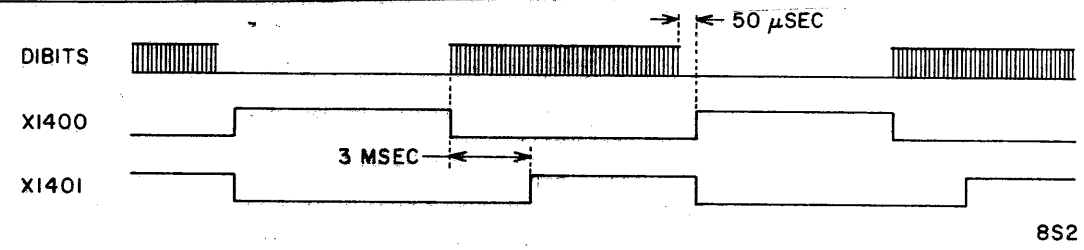
Figure 3-21. Track Servo Circuit Simplified Schematic

TABLE 3-4. TRACK SERVO CIRCUIT FUNCTIONS

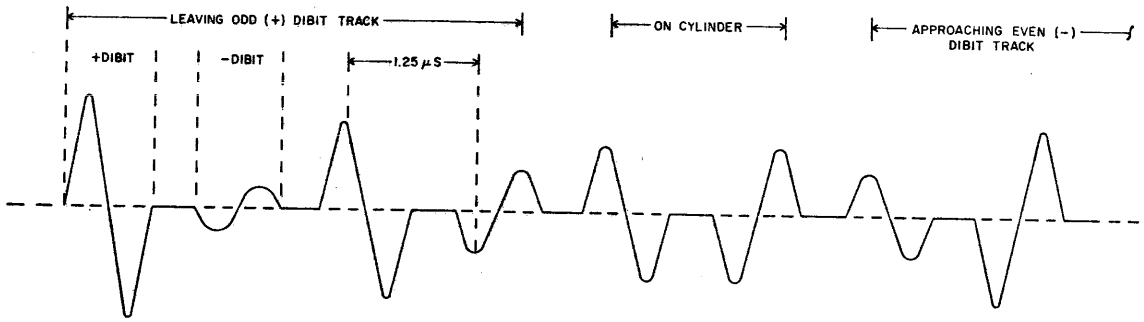
Circuit Element	Function
Track Servo Head	Reads dibit information from the disk servo tracks. This head cannot write.
Track Servo Preamplifier	Amplifies the signal read by the track servo head.
Positive and Negative Gates	Separate dibit waveforms into positive and negative components. Positive gate triggers during first half-cycle of positive dibits (read from odd dibit track) and second half-cycle of negative dibits (read from even dibit track). Negative gate triggers in the reverse condition.
Positive and Negative Delays	Function as synchronizing gates to control dibit pulses generation. Positive delay fires at leading edge of positive gate. If negative gate output is available before positive delay times out, it indicates that positive dibit has been sensed. This triggers the Odd Dibit FF. The positive gate also serves as an inhibit to the positive peak detector during the negative portion of the positive dibit and the entire negative dibit. The negative delay functions in the reverse condition.
Even Dibits and Odd Dibits Flip-Flops	Provides 600-nsec pulses indicating dibits. Frequency of each one-shot is 403 kHz.
Dibits Peak Detectors	Provide peak detection of dibit signals. Outputs are proportional to dibits amplifiers: the greater the amplitude, the more negative the output. When head is centered between dibit tracks, outputs of + and - peak detector are equal. As head moves from center position, output from one peak detector increases negatively while output from the other peak detector becomes less negative. The difference between these two outputs is proportional to servo head displacement from centered (on cylinder) position.
AGC Circuit	AGC voltage is proportional to sum of dibit signals. As signal strength increases, voltage goes less negative to reduce circuit gain.
Track Servo Amplifier	Provides signal proportional to sum of + and - dibit peak detectors. Output is null when head is centered between dibit tracks (on cylinder); negative when over odd track or outer guard band; positive when over even track or inner guard band.
Cylinder Pulse Detection	Provides cylinder pulses to difference counter and other logic elements as track servo signal approaches null. One pulse is generated per track crossed (even/odd transition or odd/even transition).
Velocity Integrator	Provides ramp signal proportional to distance travelled (velocity integrated with time). Output is positive-going during forward seek; negative-going during reverse seek. Output is pulled back to zero to re-initiate integrator function by each cylinder pulse, or during certain conditions of RTZ or Load sequences.
Dibits Detect	50 μsec and 3 ms delays used to prevent the track servo circuit from being turned on by random noise spikes during a heads unloaded condition or a load heads operation.

TABLE 3-4. TRACK SERVO CIRCUIT FUNCTIONS (Cont'd)

Circuit Element	Function
End of Travel (EOT) Detection	Monitors integrated velocity to enable EOT circuit. When velocity integrator output exceeds about 1.2v, heads have moved a distance of approximately two tracks without sensing any cylinder pulses.
Reverse EOT FF	Indicates that heads are positioned over outer guard band. Refer to First Seek and RTZS discussions for further details.
Forward EOT FF	Indicates that heads are positioned over inner guard band. This is an error condition.



Dibits Detect



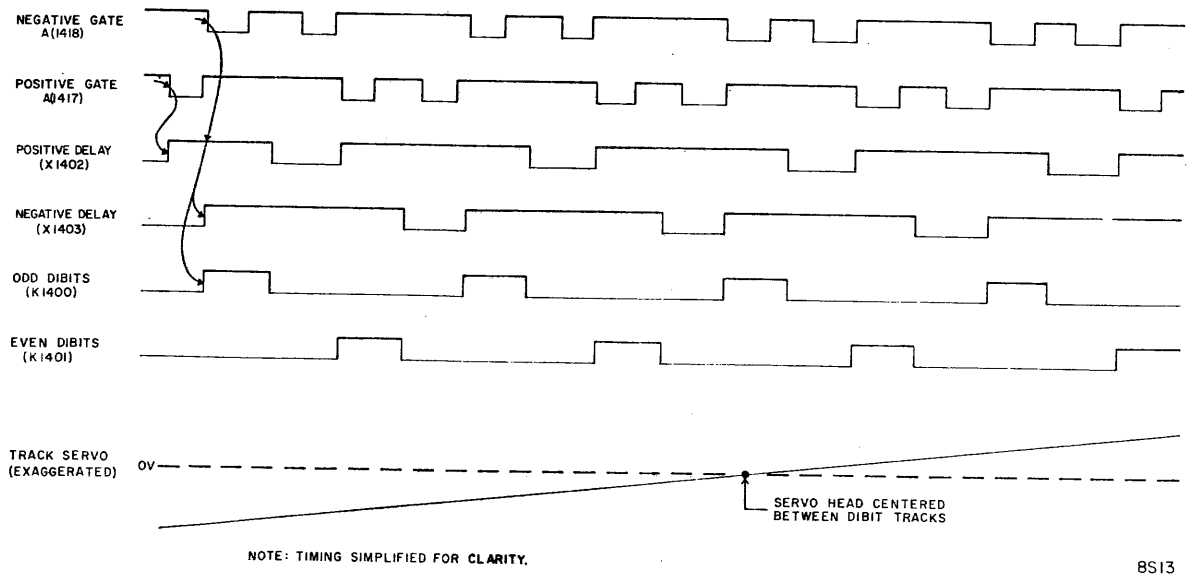


Figure 3-22. Track Servo and Dibits Detect Circuit Simplified Signals

Circuit gain control is achieved by applying the outputs from the peak detector buffers to the AGC summing amplifier. Its output is negative in proportion to signal strength: the stronger the signal, the less negative the AGC voltage. This signal is fed back to the AGC amplifier to control the resistance of a FET within the amplifier. The FET is connected across the differential inputs to the amplifier. The less negative the AGC, the less the resistance; therefore, more of the signal from the track servo head is shunted by the FET to reduce circuit gain.

The Dibits Detect FF's (X1400, X1401), prevent the circuit from being turned on by random noise spikes while the heads are unloaded or being loaded. When the preamp output is zero, as in a heads unloaded condition X1400 is not triggered and its output is high. This holds X1401 at a logic zero. The positive and negative gates and cylinder detect circuits are now inhibited. When the heads are loaded and dibits are output from the preamp, X1400 is triggered and retriggered keeping its output at a logic zero. This releases the timing components of X1401 and after 3 ms its output goes to one turning on the Track Servo Circuit. If dibits are lost for more than 50 μsec X1400 times out and resets X1401 to a logic zero disabling the track servo circuit (see Figure 3-22).

End of Travel Detection

The End of Travel (EOT) circuit determines when the heads are positioned outside of the normal data cylinders. This function is used during Load and RTZ sequences and to indicate an error condition during a seek.

Forward EOT indicates that the heads are within the inner guard band. Assume that the controller has commanded a forward seek to an illegal cylinder past cylinder 410. Sequencing is as follows (refer to Figure 3-21).

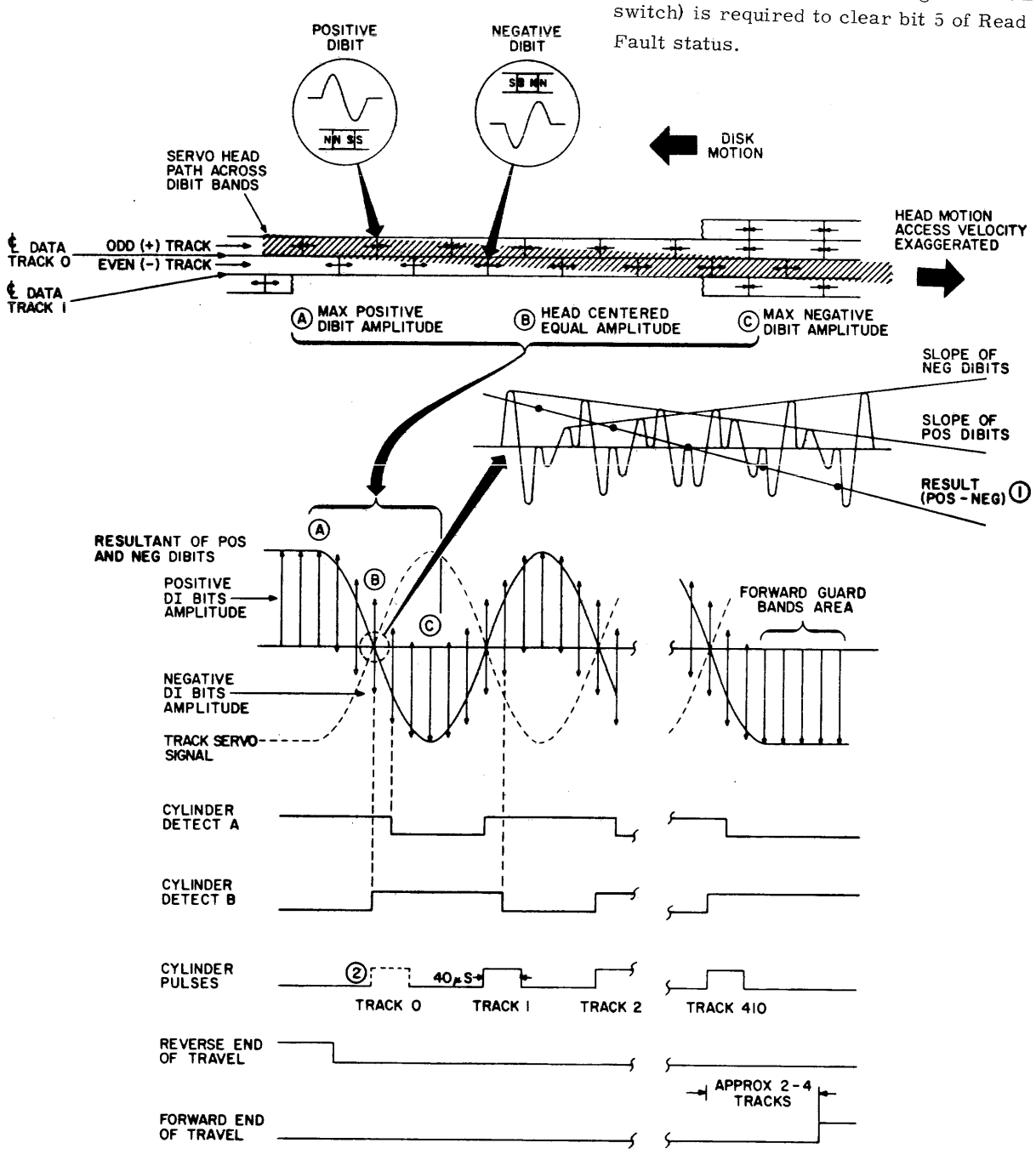
1. As the heads move forward, the velocity integrator output produces a signal proportional to velocity (the input to the integrator) and time (provided by the integrator capacitor). The output, which is a positive-going ramp during forward seeks, represents distance travelled. It is pulled back to ground by cylinder pulses. As long as cylinder pulses are generated, the output cannot reach an effective value.

2. After track 410 is passed, no more odd dibit tracks are detected, resulting in no more cylinder pulses to reset the velocity integrator. When the output exceeds approximately 1.25 volts (2-4 tracks), Forward EOT Enable comes up. This signal, in conjunction with the even dibits picked off of the inner guard band, sets the Forward EOT FF.

3. With the Forward EOT FF set:
   a. Seek FF (set at the start of the seek) is cleared. This stops the seek function. The output of the position converter in the servo circuit is blocked to indicate a zero position error.
   b. The difference counter is set to 511 (T=0).
   c. Fine Enable is raised within the servo circuit.
   d. Because of b and c, the Fine gate in the servo circuit is enabled.
   e. The Slope FF is cleared to indicate a seek to an even-numbered cylinder.
   f. The Seek Error FF sets, resulting in the remaining steps.
   g. The Seek Complete FF clears.
   h. Seek Error is raised to the controller.
   i. Bit 2 (Seek Error) is up during a Read Control Status tag.
   j. Bit 5 (Seek Error) is up during a Read Fault Status tag.
   k. Read and Write gates are disabled.

4. The track servo, functioning as the fine servo signal in the servo circuit, is gated to the servo summing amplifier via the Fine Gate. The signal is at a maximum amplitude because only even dibits are being sensed. This error voltage causes the positioner to drive in reverse until the servo signal drops to zero: the heads are then positioned at cylinder 410. The EOT FF is cleared by the odd dibits.

5. The drive will not execute any Seek, Read, or Write commands. This status requires that the controller issue a Return to Zero Seek command to clear the Seek Error. A Clear Fault signal (or pressing the FAULT switch) is required to clear bit 5 of Read Fault status.



NOTES: ① TRACK SERVO SIGNAL IS 180° OUT-OF-PHASE WITH THIS WAVEFORM.
② CYL PULSE DOES NOT AFFECT DIFFERENCE COUNTER AT TRACK 0 FOR FIRST SEEK. 7J119C

Figure 3-23. Cylinder Pulses Generation

Reverse EOT indicates that the heads are positioned over the outer guard band. If this condition occurs during regular reverse seeks, the Reverse EOT FF sets. This initiates an automatic Load sequence to return the actuator to cylinder 000. The same error condition exists, however, as if a Forward EOT occurred.

Cylinder Pulse Generation

As the servo head crosses the interface of the even/odd dibit tracks (Figure 3-23), the servo signal decreases toward null. Two operational amplifiers connected as Schmitt triggers switch state. The hysteresis designed into the circuit causes both triggers to be up only while the servo signal is between 0v and 0.4v. These signals are applied to two level shifters (L1400/L1401). Their outputs are ANDed together to provide a 40 μsec cylinder pulse. Each cylinder pulse:

1. Increments the difference counter.
2. Switches the two velocity integrators (one each in the servo circuit and track servo circuit) to ground.

It is possible that the last cylinder pulse may not be generated when the seek is completed, causing the difference counter to hang up at 510. The On Cylinder signal provides a pulse to increase the difference counter to 511.

The track servo circuit remains active following completion of a seek. If the servo head drifts off of its centered position, the track servo signal will no longer be at null. The signal, functioning as the fine servo signal within the servo circuit, will act as a position error signal to drive the positioner back into position.

FIRST SEEK

This function, also known as the Load sequence, involves the activities that a unit must perform before it can effectively respond to a Read, Write, or Seek command from the controller. This function consists mainly of power supply relay sequencing and status checking by the unit's logic. As a result, no actual selection of the unit is required and very little drive/controller signal exchange occurs. Successful progression of the function assumes that all circuit breakers are on, disk pack is installed on spindle of unit, and the interlocks are closed. Successful completion of a First Seek is signified by the occurrence of Unit Ready and the lighting of the READY indicator.

Initiation of the function occurs when the controller makes sequence power available to the power supply. Sequence power causes the power supply relay K1 to energize and the power supply performs a Power-On sequence (refer to Power supply in this section for detailed description.

See Figures 3-24 and 3-25 for first seek timing. With K1 closed, the logic enables motor relay K3. This causes release of the hysteresis brake and starts the spindle motor. At the same time, the brush motor is energized to initiate a disk cleaning cycle. Within about five seconds, the brushes move into and out of the pack area to clean the disk surfaces.

When the disk pack speed reaches 3000 rpm, the power supply relay K2 energizes to apply +20 volt power to the read/write logic and to energize retract relay K5 (the heads are unloaded) to connect the positioner voice coil to the power amplifier driven by the servo logic.

At the end of the 15-second (approximate) First Seek Interlock cycle (disk cleaning cycle in older units), the First Seek Interlock switch (brush cycle in older units) transfers and activates the first seek operation by setting the Load latch. The Load latch drives the Load gate; this bias voltage forces an average forward 7 ips access that mechanically loads the heads. The carriage continues forward with the servo head searching for the prerecorded positive dibits signals on the track servo surface. When the Reverse EOT area (all odd, or positive, dibits) is sensed, the Load latch is cleared and the Fine gate is enabled. The carriage now servoes into cylinder 000 under control of the fine servo signal.

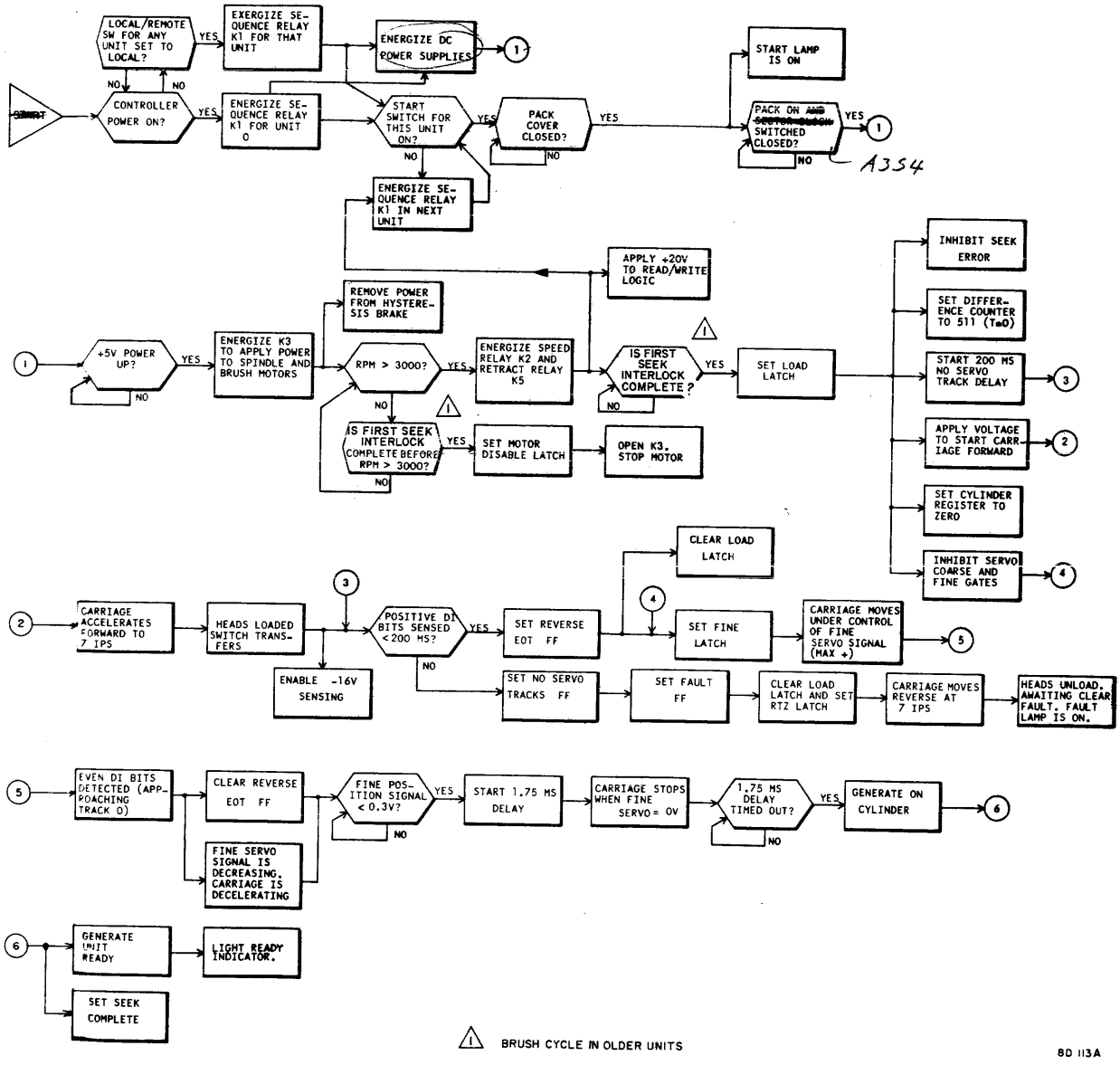
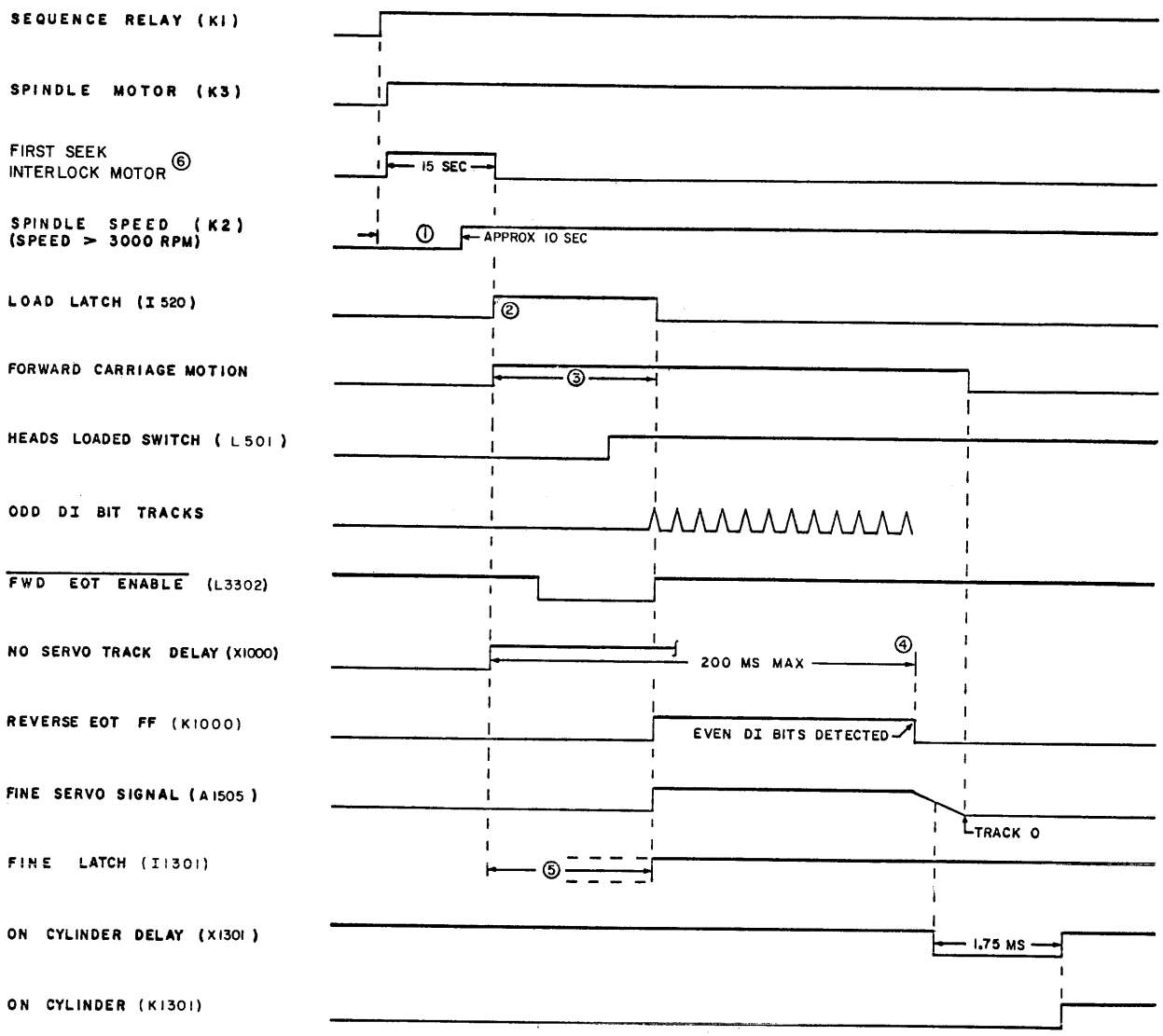


Figure 3-24. First Seek Flow Chart



NOTES:

① RETRACT RELAY K5 PICKED WHEN K2 PICKS.

② LOAD FF CAUSES LOAD GATE (A29Q3) TO APPLY + (SEEK FWD) VOLTAGE TO VOICE COIL SUMMING AMPL. COARSE AND FINE GATES INHIBITED. CYLINDER REGISTER SET TO ZERO AND DIFFERENCE COUNTER SET TO MAXIMUM (511).

③ MOTION TO 7 IPS PROVIDED BY LOAD GATE UNTIL ODD DI BITS SET REVERSE EOT FF. MOTION CONTROL THEN PROVIDED BY FINE POSITION SIGNAL.

④ DI BITS MUST BE DETECTED WITHIN 200 MS OR FAULT IS SET. HEADS UNLOAD. FAULT MUST BE CLEARED BEFORE ANOTHER LOAD ATTEMPT CAN BE MADE.

⑤ BOTH OUTPUTS ARE HIGH WHILE LOAD LATCH IS UP. THIS DISABLES COARSE AND FINE GATES, FF THEN SET BY $T \leq 1$.

⑥ BRUSH CYCLE IN OLDER UNITS

8S7A

Figure 3-25. First Seek Timing

When the positioner reaches cylinder 000, On Cylinder is generated. After a 1.75 ms delay the On Cylinder FF sets. This has the following effects:

1. Unit Ready FF sets. It can be cleared only when the heads unload.
2. Unit Ready is returned to the selected channel. The drive hardware does not require Unit Ready to accept a Unit Select.
3. The drive can accept a Control Select tag. It is ready to perform a Read, Write, or Seek operation after being selected.
4. The Cylinder register is at zero while the Difference Counter is at 511 (T=0). These resets were completed while the Load latch was set.

If, for any reason, the dibit signals are not detected by the track servo logic within 200 ms after the Load latch is set, the RTZ latch will be set. The actuator will retract to the heads unloaded position. In this case, a Fault condition exists (FAULT indicator on) to prevent reloading until the Fault is cleared. The same conditions exist if the dibits are lost for 200 ms after Unit Ready is available. Refer to Seek Status and Error Conditions for other First Seek Errors.

DIRECT (FORWARD/REVERSE) SEEK

The Direct Seek function involves those operations that must be performed to move the read/write heads from their present track or cylinder location to the one specified by the controller.

The basic principles of the seek operation are explained in the Servo Circuit discussion.

I/O Sequencing

Controller/drive signal interchanges during a seek function would be as follows (see Figures 3-26 and 3-27):

NOTE

The drive cannot recognize commands until: Cable A and Cable B interlocks are true (provided by their respective Open Cable Detectors), the drive is in On Line mode, and the drive is selected.

1. Controller issues a Cylinder Select tag.
2. Enable Counter FF sets. This enables Timing Chain Counter to increment per 806 kHz clock. Timing Chain Transfer decodes the output of the Timing Chain Counter for seek sequencing.
3. Cylinder Select clocks the desired address into the new address register.
4. The new address is inverted and added to the old address. This addition determines the following:
5. Controller places head address on output data lines and raises Head Select tag. The desired head address is loaded into the head address register.
5. Heads are deselected for a minimum of 6 μsec. They are also deselected when the actuator is not on cylinder.
7. Timing Chain Transfer decodes count 3, (not) Difference Select. Set Direction.
   a. Inverted difference count clocks into Difference Counter.
   b. Direction FF is set or cleared (set indicates a forward seek, clear indicates a reverse seek).
8. Timing Chain Transfer decodes count 5, (not) Start Seek Pulse. With unit ready

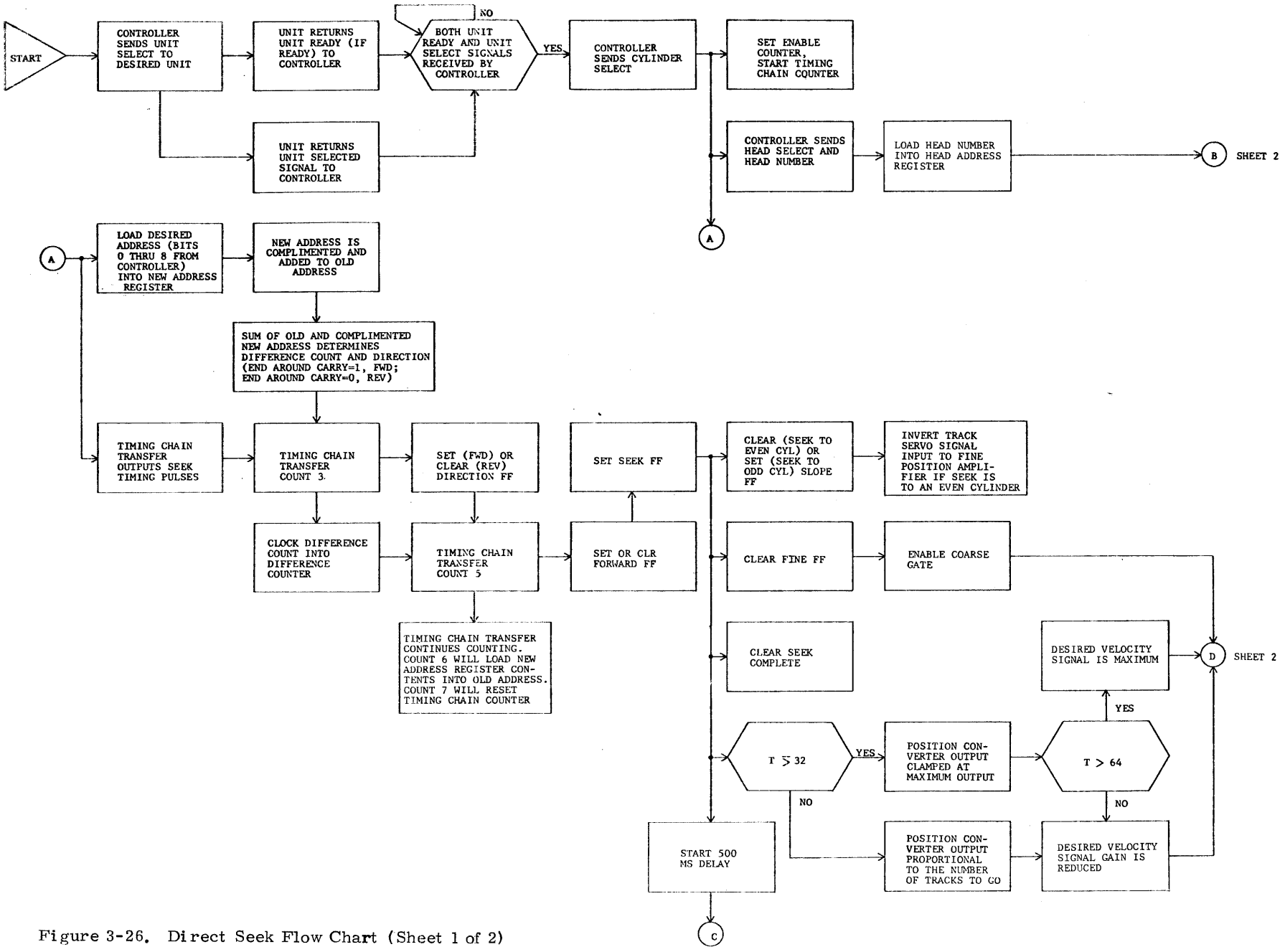


Figure 3-26. Direct Seek Flow Chart (Sheet 1 of 2)

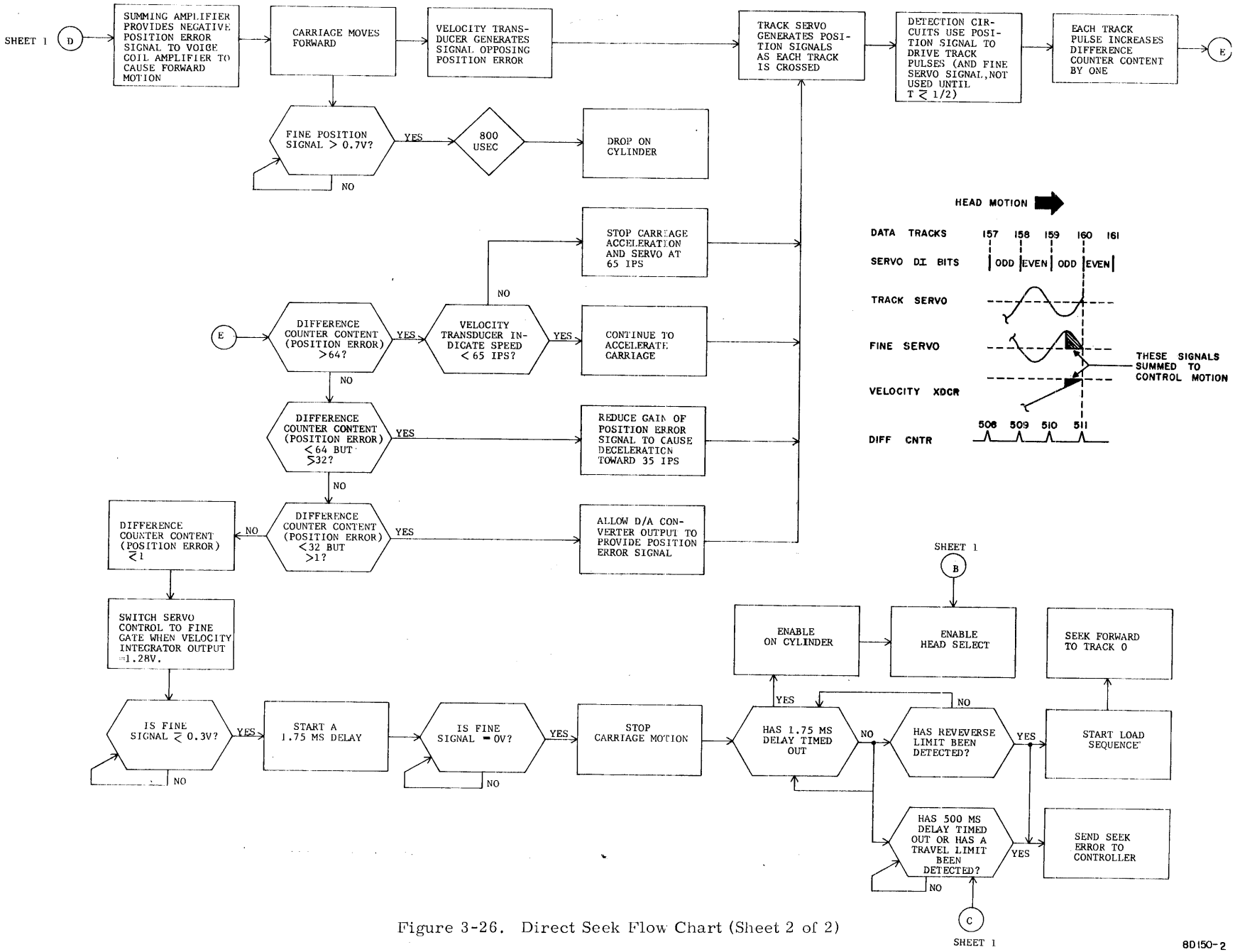


Figure 3-26. Direct Seek Flow Chart (Sheet 2 of 2)

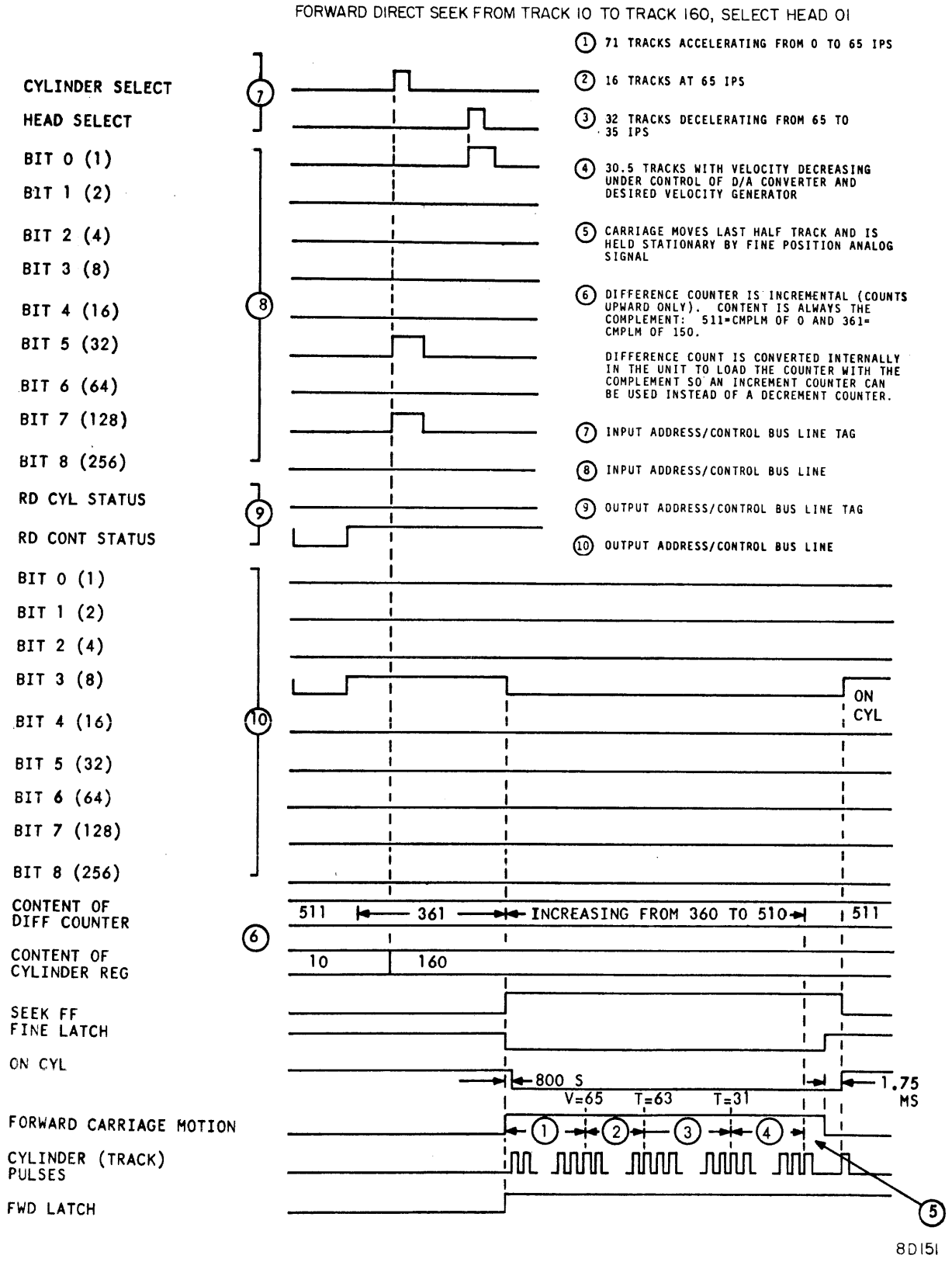


Figure 3-27. Direct Seek Timing

and no fault, the Forward FF sets (seek forward) or clears (seek reverse) and the Seek FF sets. With these FF's set:

a. Seek Complete FF clears.

b. The output of the position converter is gated to the desired velocity function generator to generate the Position Error signal. This initiates voice coil amplifier current.

c. A 1.18 ms delay is initiated. After it times out, the Cylinder Detect signals from the track servo circuit can generate Gated Cylinder pulses. These signals increment the Difference Counter.

NOTE

Once the seek is initiated, the Timing Chain Transfer continues decoding the Timing Chain Counter to prepare unit for the next seek. Count 6, (not) Load Old Address, transfers the contents of the new address register to the old address register. Count 7 (not) Reset Timing Chain, resets the Enable Counter FF and the Timing Chain Counter. With the Enable Counter FF reset, the incrementing pulses to the Timing Chain Counter are disabled and the Timing Chain Transfer is held at count 8.

9. Start Seek initiates the following events:

a. A 500 ms delay is triggered. If On Cylinder is not obtained before the delay times out, Seek Error FF sets. This inhibits On Sector and enables bit 5 of Read Fault status and bit 2 of Read Control status.

b. Bit 2^0 of Cylinder Address register is gated to the Slope FF. If this bit is up, seek is to an odd numbered cylinder. The FF will then be set. The track servo signal is, therefore, inverted before becoming the fine servo signal (position error signal when T < 1) during even seeks.

c. Fine FF is cleared. The position error signal is obtained via the coarse gate.

10. The positioner starts its seek. Refer to Positioner Motion.

11. As the positioner begins to move, the track servo signal increases. This signal functions as the fine position signal in the servo circuit. When it exceeds about 0.7v, On Cylinder Enable drops. The following events occur:

a. If On Cylinder Enable is down for more than 800 μsec, the On Cylinder FF clears, the heads are deselected.

b. The Schmitt triggers driving On Cylinder Enable have hysteresis. Fine position must exceed 0.7v to initiate Not On Cylinder while it must be less than 0.3v to enable the On Cylinder delay.

12. When the seek is completed On Cylinder is generated, a 1.2 μsec pulse sets the Seek Complete FF.

Positioner Motion

The Forward FF output gates the output of the position converter (position error signal) into the desired velocity function generator. (A Reverse FF enable would have gated an inverted position error signal). If the seek length is greater than 32 tracks, the position converter output is clamped at a fixed voltage. Receipt of the Seek Start signal also caused a Start Seek signal to occur. Start Seek clears the Fine latch, so the output of the desired velocity function generator is gated through the coarse gate to the summing amplifier. Since the carriage is stationary, no velocity signal exists to balance the position error, and forward motion of the positioner begins.

With the position error signal clamped at maximum, the power amplifier output (and voice coil positioner current) will be maximum and the positioner will continue to accelerate. As the positioner moves forward, outputs from the track servo head are processed to derive a cylinder pulse as each cylinder is crossed. Each pulse increases the content of the difference counter by one. As acceleration continues, the velocity signal opposes the position error signal by an increasing amount. The input to the

summing amplifier drops off, finally becoming zero when these opposing signals are equal. With a nulled input to the summing amplifier, voice coil current is zero. During this phase, the positioner coasts along the 65 ips plateau with the power amplifier providing only enough output voltage to compensate for the back emf of the moving voice coil positioner.

When the tracks remaining in the seek become less than 64 (difference counter decoding) the gain of the desired velocity function generator is reduced. This causes a situation wherein the velocity signal exceeds the position error signal. The servo immediately decelerates the positioner until the two signals again cancel each other. This results in a plateau (relatively short) at approximately 35 ips. The positioner proceeds on the plateau until the difference counter decoding indicates less than 32 tracks to go to the desired cylinder. At this point the position converter voltage clamp is disabled and, for the remainder of the seek (except the last track), the servo position error is derived from the D/A converter. As each track is crossed, the D/A converter output steps down by a precise and linear amount. So that the position error provided at the desired velocity function generator input is not also stepped, the integrator clamp gates the velocity integrator on between each cylinder pulse. The resulting integrator sawtooth output is added to the D/A converter output and fills in the area between the leading edges of each step. As the position error decreases, the summing amplifier control signal decelerates the positioner to keep the velocity signal/position error signal difference to zero.

When the counter indicates one track to go to the desired destination (counter=510), the integrated velocity signal is reset by the regular cylinder pulse. The integrated velocity, which indicates distance, brings up fine enable when about one-half track of travel remains. This sets the Fine latch which, in turn, enables the fine gate and disables the coarse gate.

Desired velocity no longer has an effect; the position error is supplied by the fine servo signal. This signal is the track servo signal from the track servo circuit. The amplitude of the signal is proportional to the distance between the present head position and the desired cylinder.

Since the desired destination is track 160, bit 2^0 of the Cylinder Address register is "0". This caused the Slope FF to be cleared at the start of the seek. As a result, the track servo signal is inverted to form the fine servo signal. In all seeks, the fine servo signal is phased to be opposite to the velocity signal. Since, for forward seeks, the velocity signal is positive-going from a negative value toward zero, fine servo must be negative-going toward zero so that these two signals can oppose each other.

The dibit pattern causes a track servo signal to have a positive slope while approaching an even-numbered cylinder. Therefore, the track servo signal must be inverted to serve as a usable fine servo (position error) signal. If the seek had been to an odd cylinder, Slope would have been set and the track servo signal would not have been inverted. As the positioner approaches track 160, the fine servo signal approaches 0v. The summing amplifier responds to this decrease in amplitude by decelerating the positioner so that the sum of the velocity and position error equal zero and all motion stops with the servo circuit at null.

With the Fine latch set, the On Cylinder detection circuit is enabled. It receives the analog signal from the fine position amplifier. Fine position and fine servo are equal, but 180 degrees out-of-phase. When fine position is less than about 0.3v, the read/write heads are about 0.0003-inch from nominal data track centerline. On Cylinder Enable comes up to initiate the 1.75-ms On Cylinder delay. When it times out, the On Cylinder FF sets. The heads are selected again to permit read/write operations.

Since the positioner is not locked by a mechanical mechanism, the servo circuit continues to be enabled following the seek. If the positioner should drift slightly, the track servo signal increases. This signal (fine servo), becomes a position error input to the summing amplifier. This drives the positioner back into place.

Reverse seeks function in an identical manner, except that all phases and polarities are reversed. Total seek times for forward and reverse seeks are identical for seeks of equivalent lengths.

Refer to Seek Status and Error Conditions for an explanation of status information pertaining to seek operations.

RETURN TO ZERO SEEK (RTZS)

The RTZS function is a Seek where the heads are repositioned at cylinder 000. This function is commanded when the controller issues a Control Select tag along with bit 6 (RTZ Pulse). See Figures 3-28 and 3-29 for RTZS timing.

This command is required to clear a Seek Error condition. The drive cannot respond to a RTZS command if a Fault condition exists. The Fault must first be cleared, either manually or by a Clear Fault signal, before RTZS can be recognized. RTZ is automatically executed when the ON LINE/OFF LINE/WRITE DISABLE switch is set to ON LINE. The Fault register is also cleared.

The RTZS pulse sets the RTZ latch and clears the Seek Error FF. This enables the RTZ gate; this bias voltage forces an average 7 ips reverse motion of the carriage.

When the carriage passes cylinder 000, no more even dibits are detected. This is the Reverse EOT area. The lack of even dibits inhibits cylinder pulses allowing the velocity integrator in the track servo circuit to reach a negative output in excess of 1.28v. This sets the Reverse EOT FF. The integrator is reset, but reverse motion continues unimpeded.

After an additional reverse motion of about two to four tracks, the velocity integrator output again exceeds 1.28v. The RTZ latch is cleared while the Load latch sets. The logic now functions in a manner equivalent to the First Seek sequence.

With the Load latch set, the Load gate supplies a voltage to command a 7 ips forward motion. The velocity integrator, this time indicating forward distance, clears the Load latch to permit continued motion under control of the fine servo signal. The carriage then servoes into cylinder 000.

On Cylinder is available 1.75 ms after the RTZS is completed. The sequence must be completed within 500 ms after RTZS initiation, or else Seek Error is set.

The RTZS function is also used during normal power off sequencing. When the operator presses the START switch, the control interlock opens. This raises the Unload Heads signal in the drive logic. The RTZ latch sets to initiate a 7 ips reverse seek. This time however, the EOT Enable circuit is disabled so that the velocity integrator signal has no effect. In turn, the Load latch is disabled. Reverse motion continues until the heads unload. A Fault condition does not inhibit the unloading; however, unloading does not clear the FAULT indicator.

The RTZS function occurs automatically in the heads unloaded condition if dibits are lost for more than 200 ms. The Fault FF is set to prevent another First Seek until the FAULT indicator has been cleared.

Normal Status Conditions

The following status conditions are not, in themselves, considered as error conditions. They may, however, shake up the system if there is an element of surprise in them.

On Cylinder indicates that the heads are positioned over a normal data track. This signal is generated 1.75 milliseconds after the Fine Position signal is less than about 0.3v. Seek Error status can exist at the same time. The On Cylinder signal drops when the Fine Position signal exceeds about 0.7v for more than 8 μsec: either a seek has started or there is an electromechanical error.

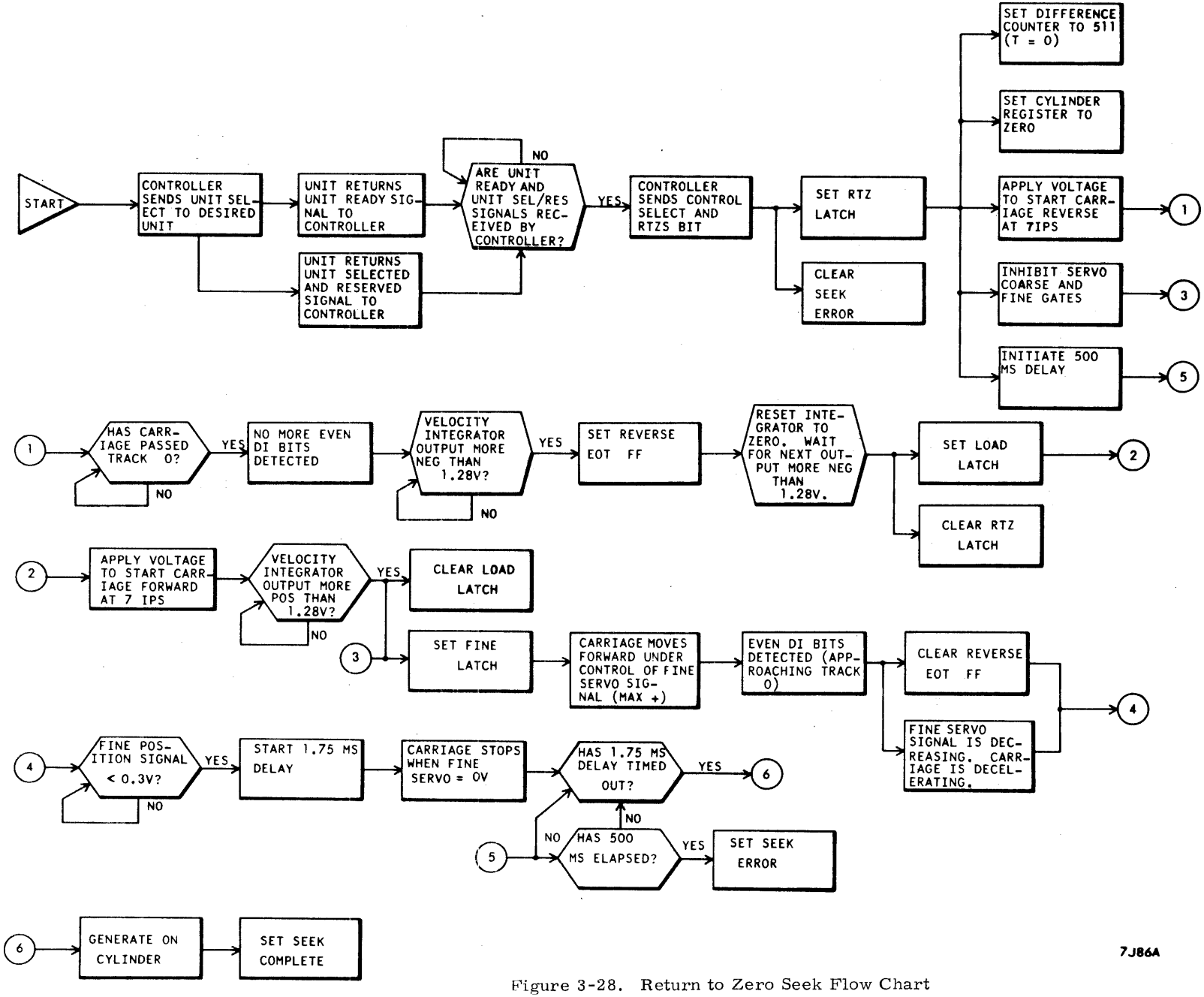
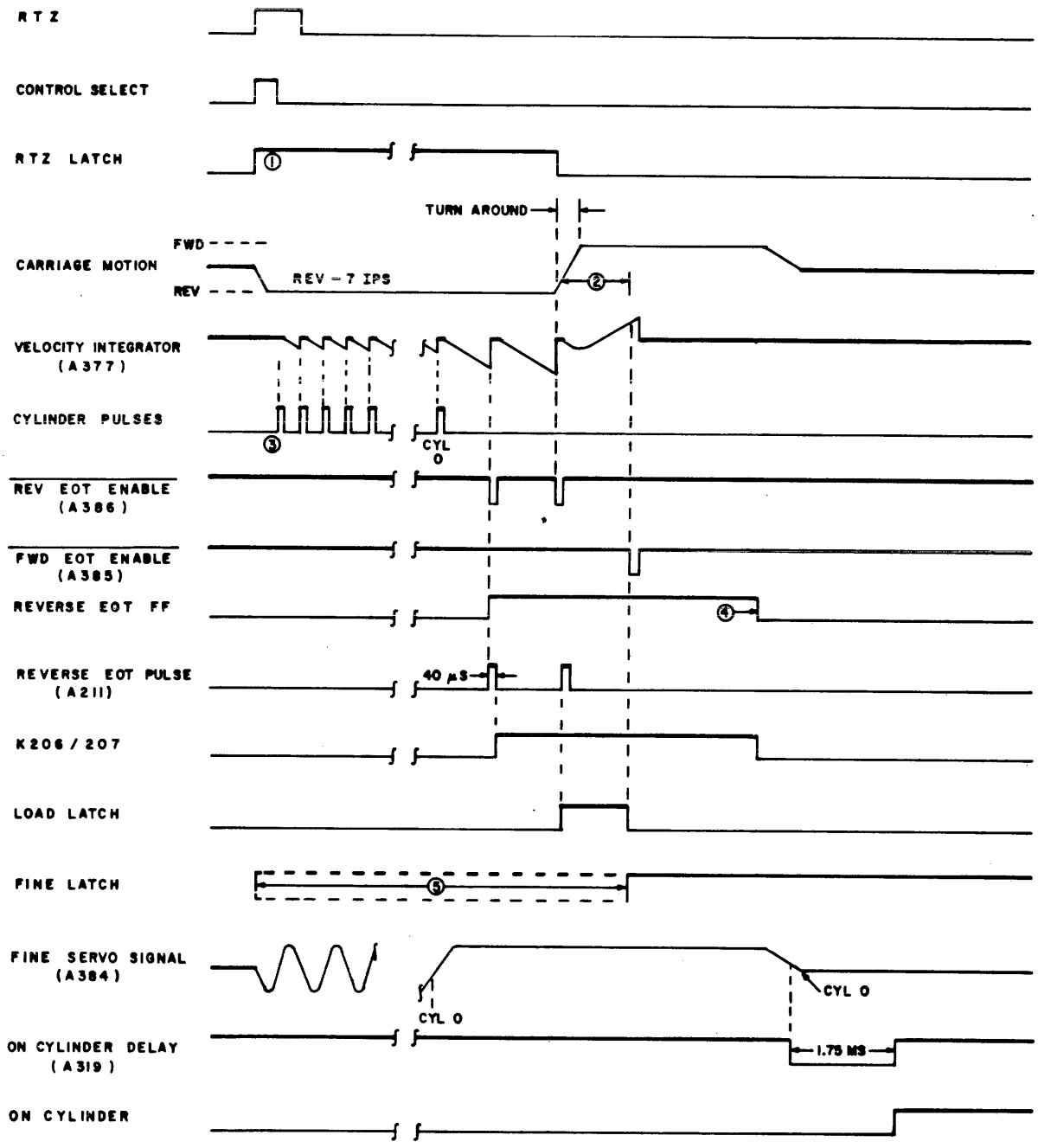


Figure 3-28. Return to Zero Seek Flow Chart



NOTES:

① RTZ LATCH CAUSES RTZ GATE (A29Q2) TO APPLY NEG VOLTAGE (SEEK REV) TO VOICE COIL SUMMING AMPL. COARSE AND FINE GATES INHIBITED. CYLINDER REGISTER SET TO ZERO AND DIFFERENCE COUNTER SET TO MAXIMUM (511)

② FWD MOTION TO 7 IPS PROVIDED BY LOAD GATE (A29Q3) -- IT PROVIDES + (SEEK FWD) TO SUMMING AMPL. WHEN LOAD LATCH CLEARS, MOTION CONTROL PROVIDED BY FINE SERVO SIGNAL.

③ CYLINDER PULSES RESTART VELOCITY INTEGRATOR. THEY DO NOT AFFECT DIFFERENCE COUNTER.

④ REVERSE EOT FF CLEARED BY FIRST EVEN DI BITS. (APPROACHING TRACK 0).

⑤ BOTH OUTPUTS ARE HIGH WITH EITHER RTZ OR LOAD LATCH SET. THIS DISABLES COARSE AND FINE GATES. FF THEN SET BY T ≤ 1.

7J85A

Figure 3-29. Return to Zero Seek Timing Diagram

End of Cylinder (Read Control Status bit 6) is generated whenever the Head register contains a value of 18 or greater. This can result from a tag Head Advance with the Head register already at 18.

Error Status Condition

The following status conditions are generally considered as being drive or interface errors.

Seek Error (via the "A" Cable) indicates that one or more of the following errors occurred:

1. Drive could not complete a seek (including RTZS) within 500 ms following receipt of a seek command.
2. Drive went Off Cylinder for more than 500 μsec during a non-seek condition (that is, after the initial 500-ms timeout). Off Cylinder occurs when the Position Servo signal exceeds about 0.7v (700 microinches off of the track centerline).
3. Heads went into the Forward EOT area or (except during RTZS functions) the Reverse EOT area.

Seek Error is also indicated during two status tags. It is bit 2 of Read Control Status and bit 5 of Read Fault Status. A Return to Zero command (Control Select bit 6) clears Seek Error and bit 2. The bit 5 error, since it is stored in the drive Fault register, also requires a Clear Fault following the RTZS.

End of Travel (Read Position Status bit 3) is up while the heads are still in the Forward EOT or Reverse EOT area. The signal drops when the heads are repositioned at cylinder 000 (following a Reverse EOT) or at cylinder 410 (following a Forward EOT). If the drive is not processing a First Seek or RTZS sequence, Seek Error is also set.

Any of the following errors are hardware faults. The Fault FF is set to inhibit execution of any commands until a Clear Fault has been issued.

This raises a flag on the fault line to the controller, Bit 1 (pack unsafe) of read control status is true, and the fault indicator is lighted.

1. If Write Gate (Control Select bit 0) or Read Gate (bit 1) is raised while the heads are not On Cylinder, Read Fault Status bit 0 is true.
2. If the -16v emergency retract voltage becomes insufficient, Retract relay K5 opens to retract the heads to the unloaded position. Another voltage sensing circuit sets Read Fault Status bit 4 (- volt).

MACHINE CLOCK CIRCUIT

The machine clock circuit uses dibits generated by the track servo circuit to generate the basic 806 kHz clock signal. This signal is applied to the following circuits:

1. Index detection
2. Seek Timing Chain

Clock Generation

The circuits (Figure 3-30) most important portion is a phase locked loop (PLL). The loop compares the frequency of input data (dibits) with feedback data. A comparator circuit generates a square wave input to a GJK circuit in the voltage controlled oscillator. (Refer to Logic Card manuals for an explanation of the GJK circuit.) The GJK generates a voltage proportional to the difference in frequency between input data and feedback data. The output of the GJK is applied to the voltage controlled oscillator to control its frequency. The PLL is satisfied when the input and feedback frequencies are identical. Note that data and feedback are 90 degrees out of phase.

There are three inputs to the comparator. One is the normal input from dibits delayed approximately 1/4 cell and shaped to 30 nsec (approximate) pulses. The second input is a dub-in input. This is a 30 nsec pulse coming up at the same time as the normal input but from the clock output. The third input is the reset pulse. It is the normal and the reset input which provide the basis for normal comparator operation.

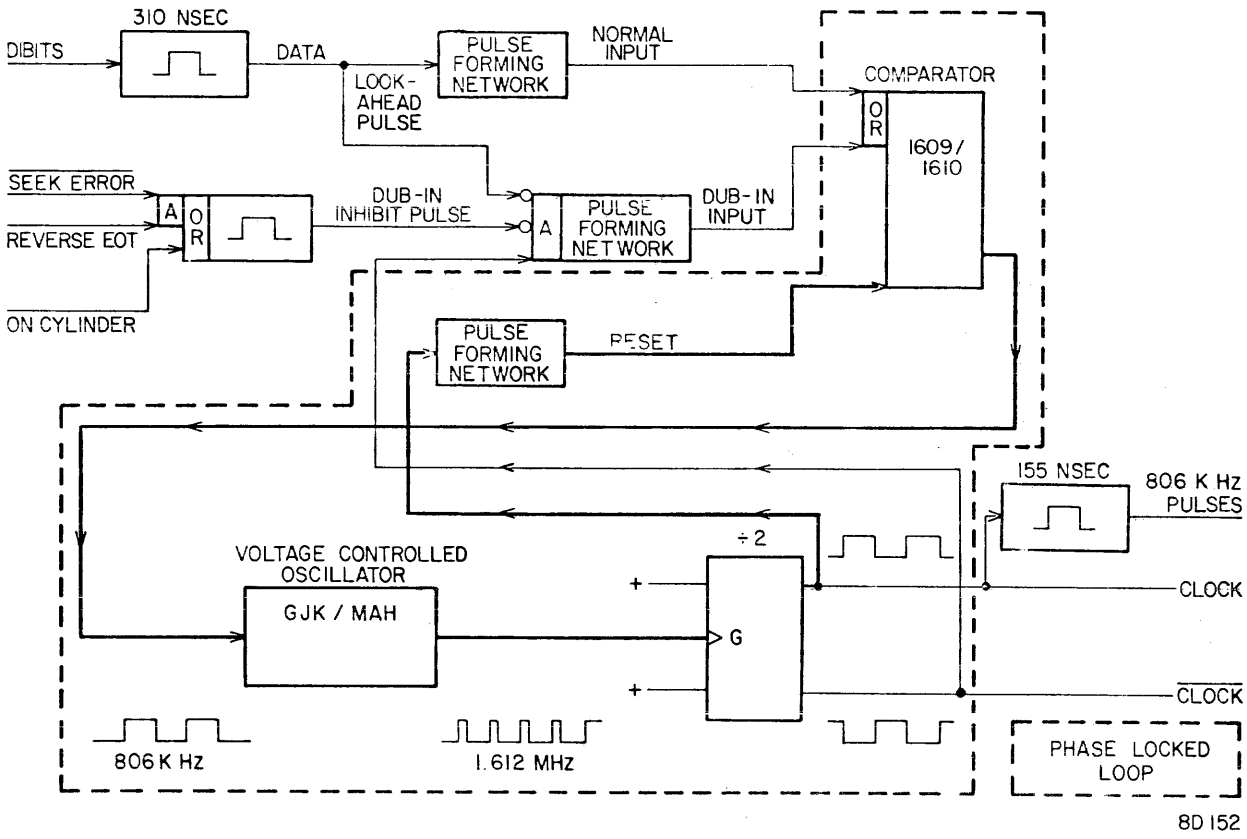


Figure 3-30. Machine Clock Circuit

During normal operation, a look-ahead pulse blocks the dub-in input to the comparator. This insures that the comparator and therefore the clock, tracks with the read input data from dibits. However, if dibits are missing, as they are during the Index mark (for two cells) or during a seek (every other cell) there must be a pseudo-dibit or dub-in pulse to keep the clock in phase. Therefore, the circuit is self-ringing when data is not present at the input.

A problem with the self-ringing feature of the circuit is that, if the first input to the comparator is not data but a dub-in pulse, the circuit may not be in synchronization with real data when it is received. It would then take some time before synchronization could be attained. The 5 ms dub-in inhibit pulse fires to block dub-in pulses in three situations; 1) When the latch is cleared by reverse EOT at the end of a first seek, or 2) and 3) When On Cylinder is received after a forward or reverse seek error.

After the heads are loaded, even/odd dibits are available. Their nominal frequency is 806 kHz. The actual frequency is a function of spindle motor speed. The PLL quickly synchronizes itself to the actual dibit rate. This permits the clock to react to variations in spindle speed between drives. Signals derived from this circuit, such as sectors, are a function of actual spindle speed rather than functions of an absolute time base.

FF K1601 is connected as a divide-by-two circuit. This circuit arrangement permits the PLL feedback to be a function of negative-going edges of the PLL output. Therefore, PLL unsymetrical outputs are ignored and the basic frequency is the controlling factor. The PLL output frequency is nominally 1.612 MHz.

Index Detection Circuit

The Index detection circuit (Figure 3-31) generates a 2-μsec pulse at the start of each new logical track. This signal is returned to the controller as Index (Control Status Bit 4).

Prior to reaching the Index area, both even and odd dibits are available. Dibits Present FF (K1700) is held in its preset state: this causes the counter (S1700) to be continually reset. The counter can increment only if the precise Index pattern is sensed. Any other combination of missing dibits (such as when tracks are crossed during seeks) will cause the counter to reset to zero.

When the counter reaches a decoded value of 6, a 2 μsec index pulse is generated. When the next even dibit occurs, the counter is again reset. Because Dibits Present FF is set and the counter output is decoded zero, the counter remains reset until the next index pattern of missing dibits.

Sector Pulse Generation

The sector circuit permits the controller to determine the current angular position (sector) of the read/write heads with respect to Index. Each track may be considered as subdivided into 24 segments. They are numbered from 00 to 23. Sector 00 is the first sector following Index.

The circuit has two major elements:

1. A clock counter to count even clock pulses.
2. A sector counter that maintains a continuous count of the current sector.

The Even Dibits FF (K1700) is used to increment the clock counter and thereby generate the sector count.

The Index pulse clears the sector counter and sets (K1701). The next even clock pulse presets the clock counter to 116. (See Figure 3-32). The clock counter advances on every even clock pulse until it reaches a count of 255. This enables Sector X2 (I1705) which increments the sector counter to 1. The next even clock pulse again presets the clock counter to 116. Note that at this point the outputs from the sector counter and K2600 are such that I2605 is not enabled.

The clock counter continues to count even clock pulses until it again reaches a count of 255. Sector X2 is enabled incrementing the sector counter. However this time I2605 outputs a sector pulse to the controller.

The sector counter will be advanced every time the clock counter reaches 255 until it is reset by the Index signal. The output of the sector counter can be monitored by the controller.

BASIC READ/WRITE PRINCIPLES

Introduction

Information is recorded on, and read from, the disk pack by means of 19 heads. Each head contains a read/write coil.

Writing Data

Data is written by passing a current through a read/write coil within the selected head. This generates a flux field across the gap in the head (Figure 3-33). The flux field magnetizes the iron oxide particles bound to the disk surface. Each particle is then the equivalent of a miniature bar magnet with a North pole and a South pole. The writing process orients the poles to permanently store the direction of the flux field as the oxide passes beneath the head. The direction of the flux field is a function of Write current polarity while its amplitude depends on the amount of current: the greater the current, the more oxide particles that are affected.

Information (data) is written by reversing the current through the head. This change in current polarity switches the direction of the flux field

across the gap. The flux change defines a data bit.

Erasing old data is accomplished by writing over any data which may already be on the disk.

Reading Data

As the disk passes beneath the read/write head, the stored flux intersects the gap (Figure 3-34). Gap motion through the flux induces a voltage in the head windings. This voltage is analyzed by the read circuit to define the data recorded on the disk. Each flux reversal (caused by a current polarity change while writing) generates a readback voltage pulse. Each pulse, in turn, represents a data bit.

Track Format

Each track has Index as its starting point. Index signal is available to the controller.

One track is operated upon by one read/write head. The heads are numbered from 0 to 18. These heads are positioned vertically with respect to each other. As a result all 19 of the heads may be used without moving the actuator. Since any of the heads may be addressed at practically instantaneous rates, the recording medium may be thought of as a cylinder rather than as 19 discrete surfaces. This is the cylinder concept. Since the actuator may be positioned horizontally to any one of 411 rings or tracks,

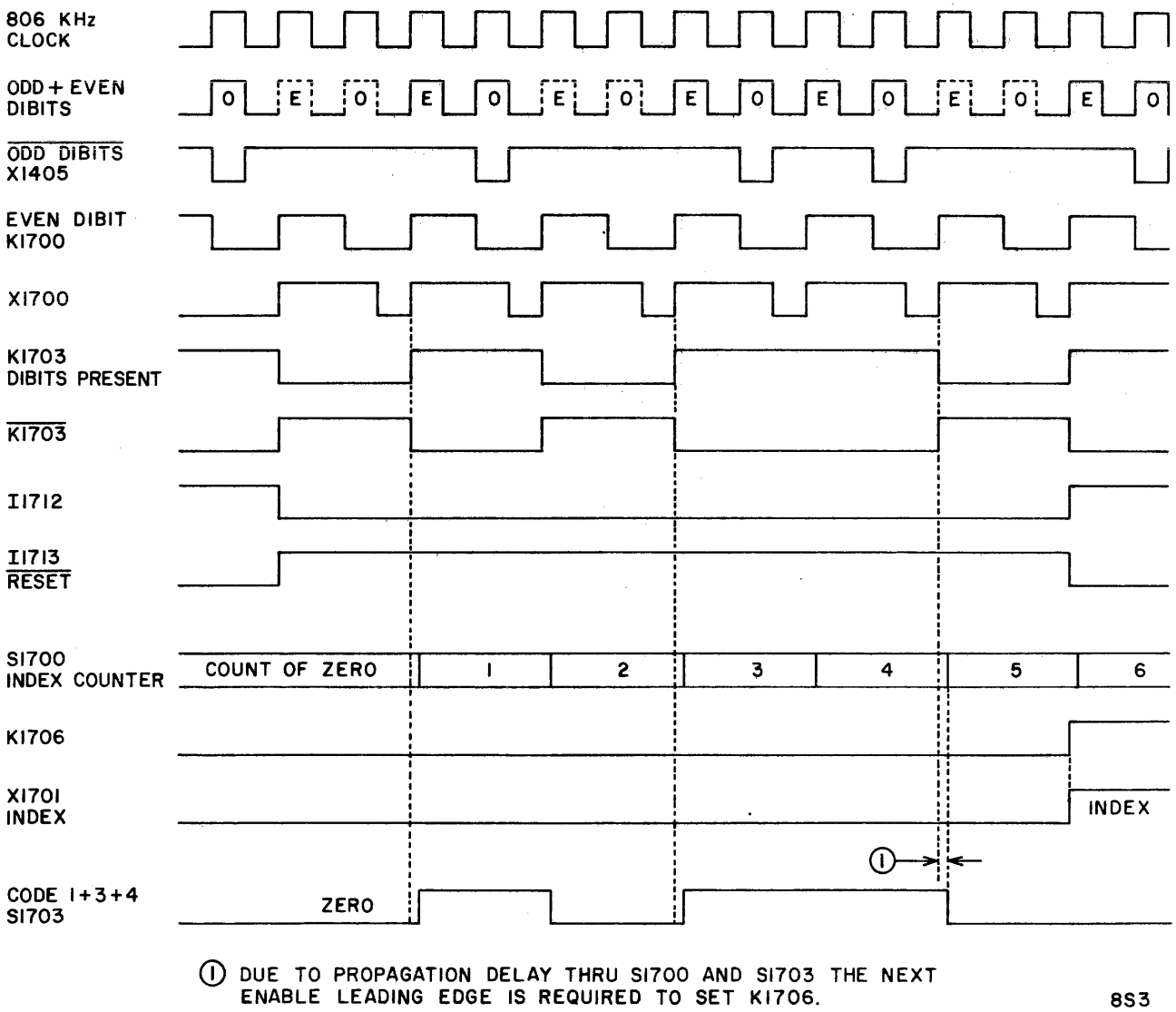
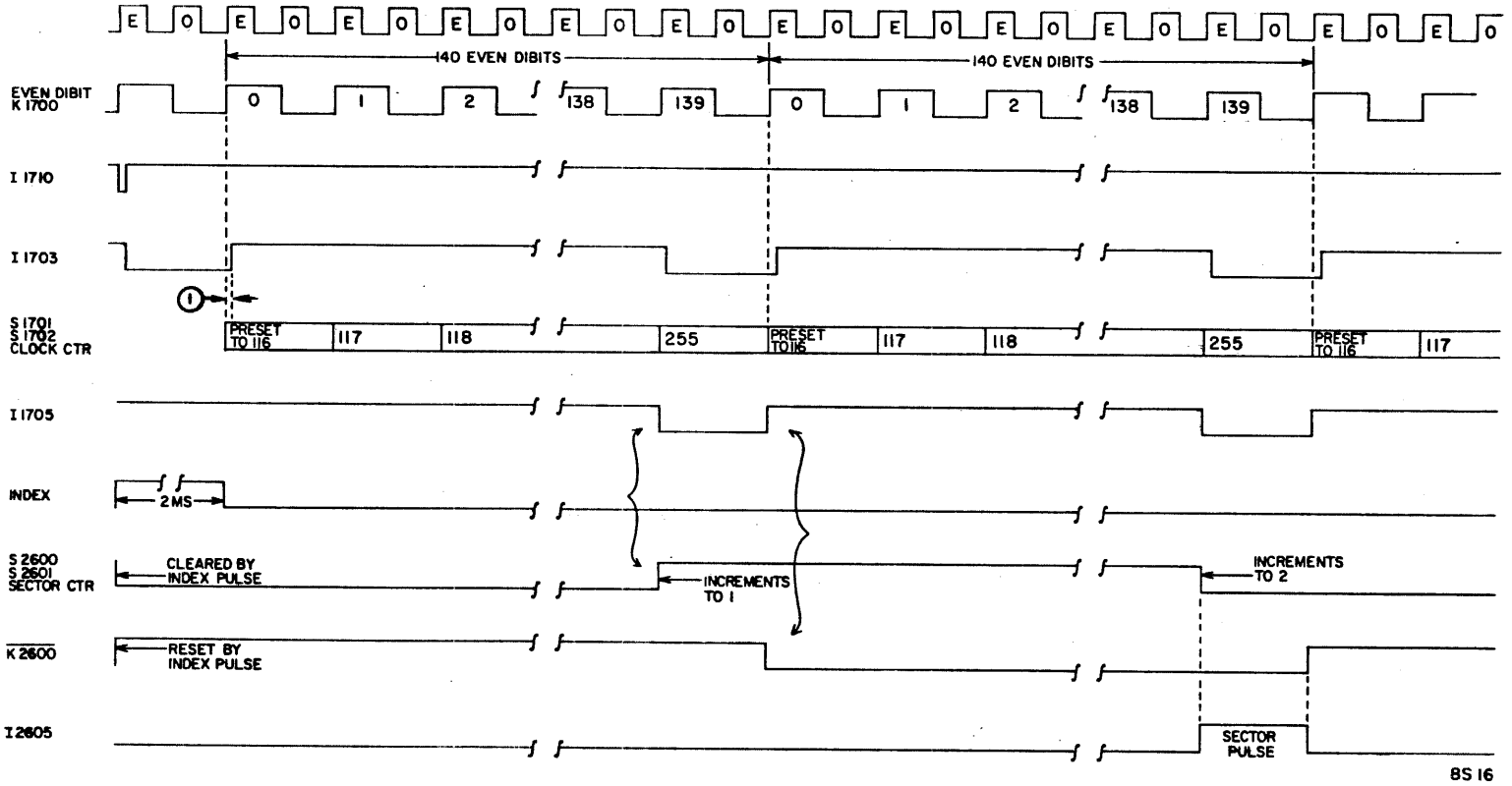


Figure 3-31. Index Detection Timing Diagram



① Propagation Delay due to K1701, I1702, I1703

Figure 3-32. Sector Pulse Timing

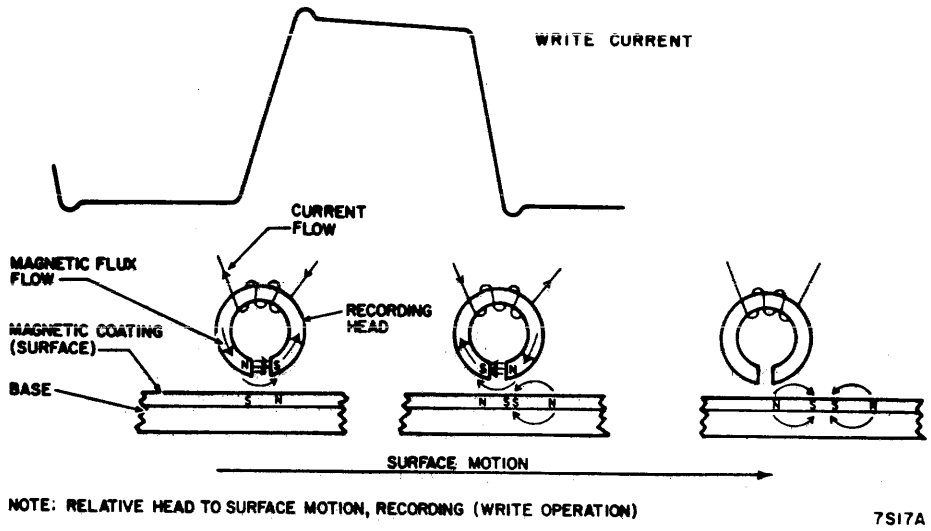


Figure 3-33. Writing Data

there are 411 cylinders. They are numbered from 000 (the cylinder nearest the outside edge of the disk) to 410 (the innermost cylinder). Any track may be address by seeking to the desired cylinder and by selecting one head. Only one head may be selected at a time.

Track format and data record format are functions of the operating system. These functions are directly controlled by the controller. Refer to the applicable controller manual for further information.

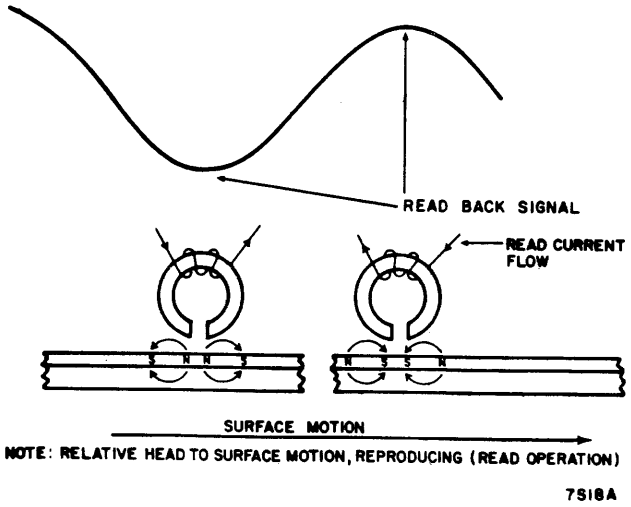


Figure 3-34 Reading Data

Principles Of MFM Recording

In order to define the binary digits stored on the pack, the frequency of the flux reversals must be carefully controlled. Several recording methods are available; each has its advantages and disadvantages. This unit uses the Modified Frequency Modulation technique.

The length of time required to define one bit of information is the cell. Each cell is nominally 147 nsec in width. The data transfer rate is, therefore, nominally 6.8 MHz.

MFM defines a "1" by writing a pulse at the half-cell time (Figure 3-35). A "0" is defined by the absence of a pulse at the half-cell time. A pulse at the beginning of a cell is Clock; however, Clock is not always written. Clock is suppressed if there will be a "1" in this cell or if there was a "1" in the previous cell.

The rulse for MFM recording may be summarized as follows:

1. There is a flux transition for each "1" bit at the time of the "1".
2. There is a flux transition between each pair of "0" bits.

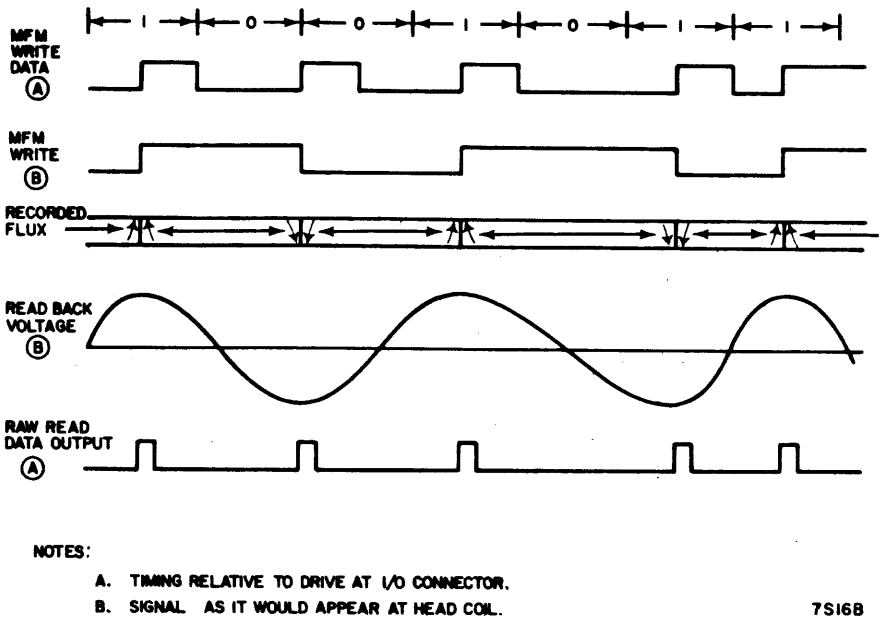


Figure 3-35. MFM Recording

3. There is no flux transition between the bits of a "10" or "01" combination.

The advantages and disadvantages of MFM recording are as follows:

1. Fewer flux reversals are needed to represent a given binary number because there are no flux reversals at the cell boundaries. This achieves higher recording densities of data without increasing the number of flux reversals per inch.

2. Signal-to-noise ratio, amplitude resolution, read chain operation, and operation of the heads are improved by the lower recording frequency achieved because of fewer flux reversals required for a given binary number.

3. Pulse polarity has no relation to the value of a bit without defining the cell time along with cell polarity. This requires additional read/write logic and high quality recording media to be accomplished.

READ/WRITE OPERATIONS

Introduction

An overall block diagram of the read/write chain is shown in Figure 3-36. More detailed block diagrams and timing diagrams are shown in conjunction with the discussions of the various stages in the read/write chain.

Head Selection

The Head Select circuit must select the desired head before a Read or Write operation can be performed. The head selection process is initiated by a Head Select tag from the controller. This tag gates the desired head address into the Head Address register (Figure 3-37). For purposes of this discussion, assume that head 16 is the head to be selected. Also assume that the present head selected is head 00.

The controller places the address for head 16 (10000) on the 5 low order bits of the address and control bus lines. The Select Head tag is then transmitted to the

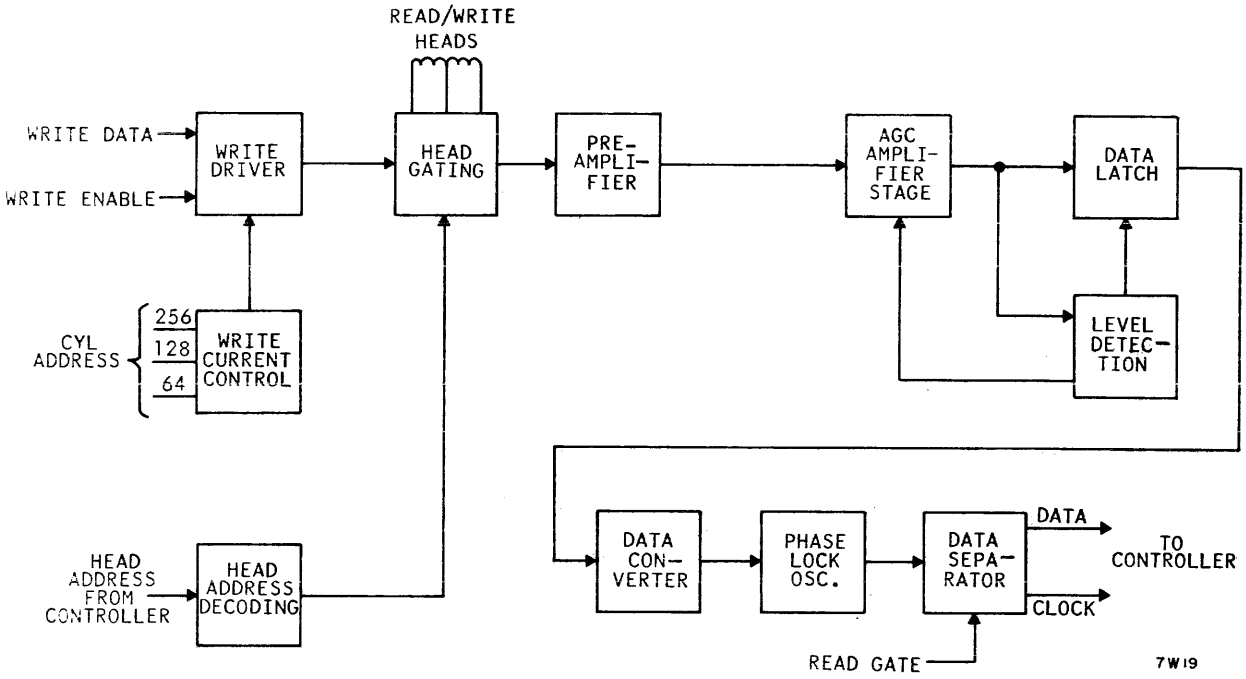


Figure 3-36. Read/Write Chain Block Diagram

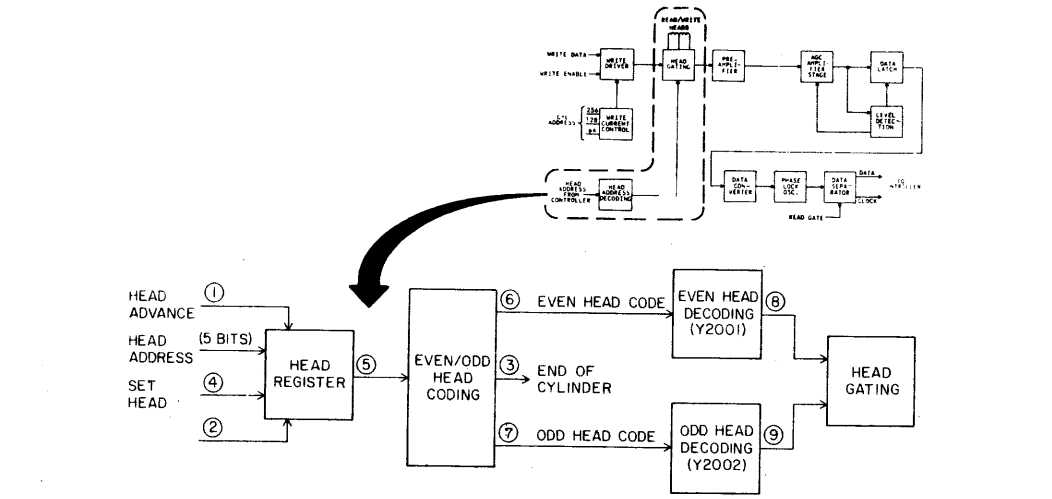
unit. This generates a Not Head Select signal at I1810 (Figure 3-37) that gates the address information into the Head Address register. At this time, a Deselect Heads signal is generated by I1901 to disable all heads for 6 μsec. This ensures that a multiple head fault is not generated during the switch in addresses and gives the head register time to stabilize. The Deselect Heads signal is also generated when the unit moves off cylinder. In this case, the signal remains up as long as the unit is in an off cylinder condition.

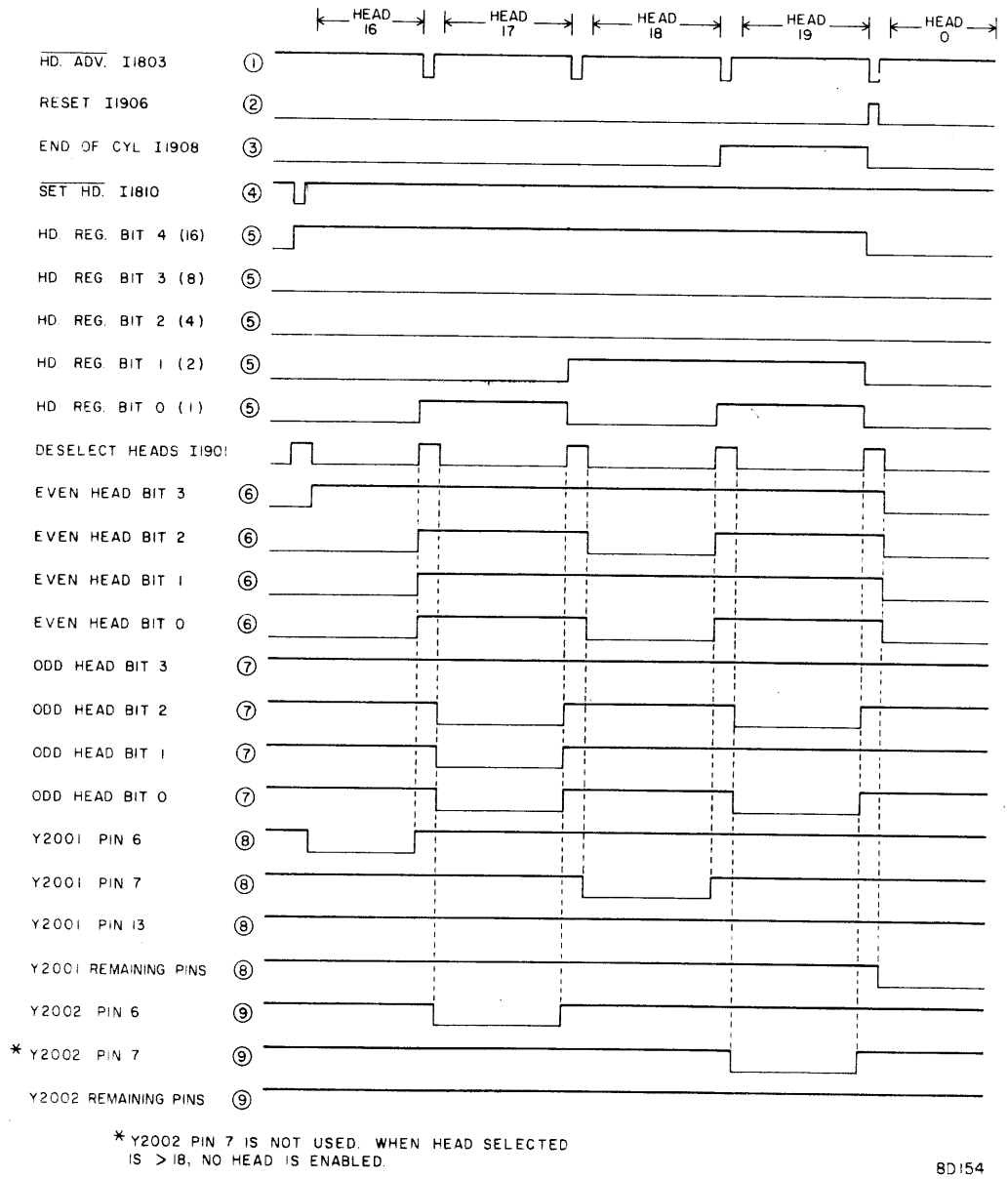
The even/odd head coding chain (I1909 through I1928) is enabled after the 6-μsec Deselect Heads signal drops. Refer to the waveforms in Figure 3-37 to follow the decoding process. The end result generates a "0" output on pin 6 of Y2001 to select head 16. The remaining pins on Y2001 and all pins on Y2002 have "1" outputs to disable their respective heads. The output from pin 6 of Y2001 grounds the center tap of head 16 through the VHJ/VHK circuitry.

The content of the Head Address register can be increases in increments of one by a Head Advance signal from the controller. If head advance is true, one of the following occurs: If current head address is less than 18, the head address will advance one count; if current head address is equal to 18, the head address will advance one count and End of Cylinder is generated; if current head address is greater than 18, an End of Cylinder exists and the Head Address register is reset to zero.

Write Data Processing

A Write operation actually begins before the voice coil positioner moves the heads to the desired track. The Head Select tag gates the identifying number of the head to be used into the Head Address register (see Head Selection description). When the seek operation is completed, the unit sends an Interrupt signal to the controller. This signal informs the controller that the unit is On Cylinder and ready to receive further commands.





* Y2002 PIN 7 IS NOT USED. WHEN HEAD SELECTED IS > 18, NO HEAD IS ENABLED.

8D154

Figure 3-37. Head Select Timing

The controller now examines the Seek Error and On Cylinder lines. If a Seek Error exists, the controller sends a Restore function code to clear it. If an On Cylinder exists, the controller responds with a Control Select and bit 1 of the address and control bus (Read Gate) to the unit. This enables the Read circuit logic function with the previously selected head to read the data record on the disk pack. The address is read from the Read Data line by the controller and compared with the address of the desired record. If the address is correct, the controller drops Read Gate and brings up Write Gate (bit 0)with a Control Select function code. This disables the Read circuit and enables the Write circuit.

Assume that the unit is selected. The write data is transmitted to the unit and applied to differential receiver L2305 (Figure 3-38). The data is processed through L2305, line driver T2300, and applied to differential receiver L2300. Write Enable must now be up if the data is to continue along the write chain. The Write Enable signal is generated if the following signals are true: On Cylinder, Write Gate, and Not Write Disable switch. If Write Enable is up, the data is allowed to pass through the remainder of the chain to the selected head and is written on the disk pack.

Discrete component circuit QEL (X2301) restores to the data signals the symmetry that may have been lost in the write chain. Refer to the Maintenance Aids section (see Preface) for a detailed description of this circuit.

Read Data Processing

AGC Amplifier Stage

The analog read data from the read head is passed through the preamplifier and applied to a low pass filter in the AGC amplifier stage (Figure 3-39). This filter attenuates the high unwanted frequencies (noise) in the read data signal and provides a linear phase response over the read data frequencies.

The output of the filter is applied to the AGC amplifier (A2401). The AGC amplifier provides a relatively constant output from a wide amplitude range on the input. This is accomplished by the AGC Control circuit which varies the gain of the AGC amplifier as the output varies.

The output of the AGC amplifier is amplified and differentiated and then applied to the Data Latch and Level Detection circuits.

Level Detector and Time Constant Control

The Level Detector and Time Constant Control circuit contains an amplitude enable pulse generator, a data detector to detect the address mark gap, and a circuit to control the time constants of the AGC amplifier and level detector.

The output of the differentiator (Figure 3-40) is applied to a filter (A2500) which attenuates the third harmonic of the low frequency Read signal. This effectively lowers the resolution of the signal.

The output of the filter is amplified and then rectified. A capacitor is charged to the average dc level of the rectified signal. This voltage is then applied to the reference input of a comparator (A2504) and the rectified signal to the other input. When the rectified signal becomes more positive than the reference signal, the comparator switches. This produces a squarewave output that is used as an Amplitude Enable signal to reject noise and spurious pulses in the address gap area. The only time this output is used is during a Search Address Mark Operation.

The Data Detector consists of a comparator (A2502) and a retriggerable single shot delay (X2502). The reference voltage on the comparator is a fixed dc

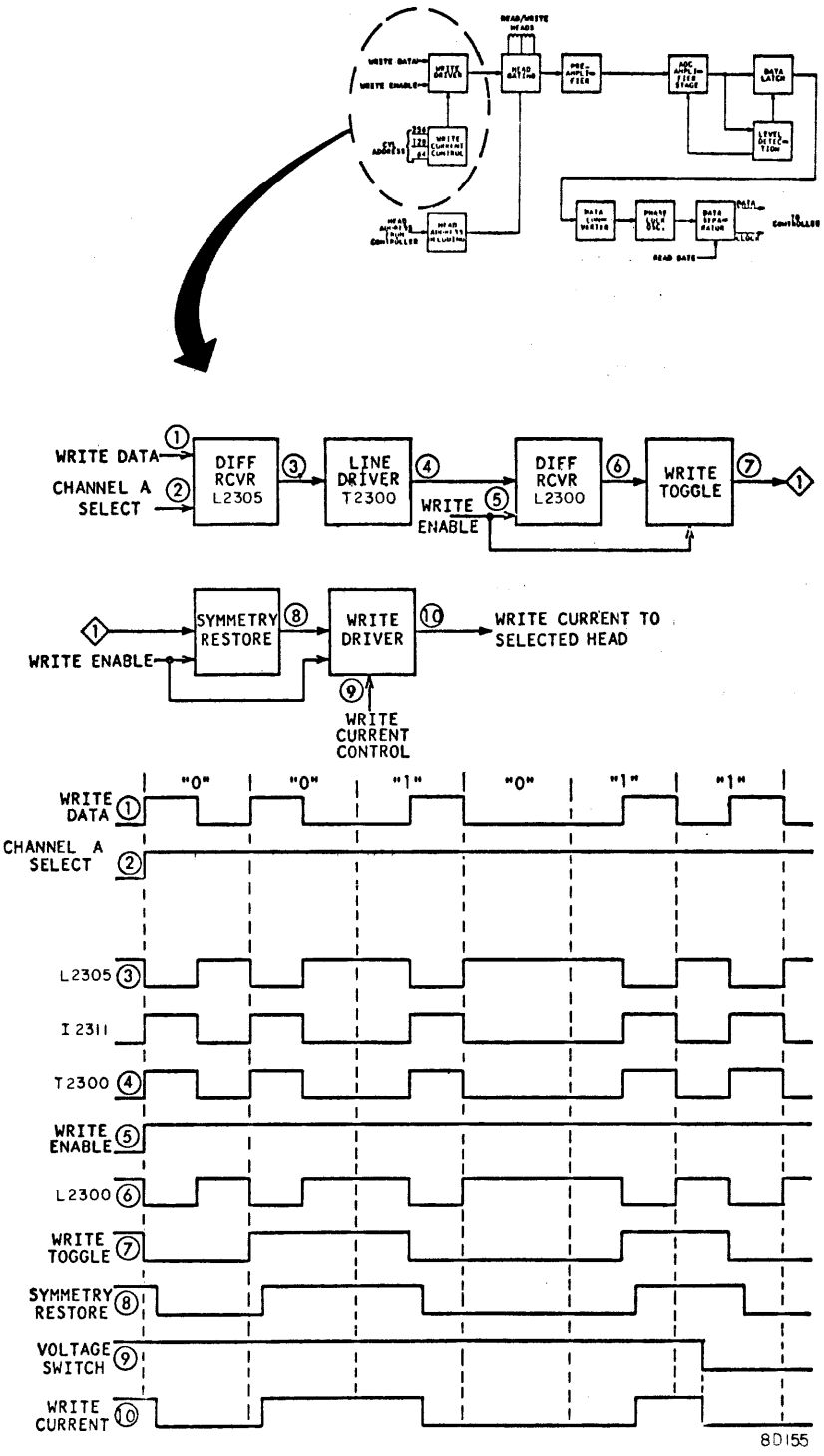
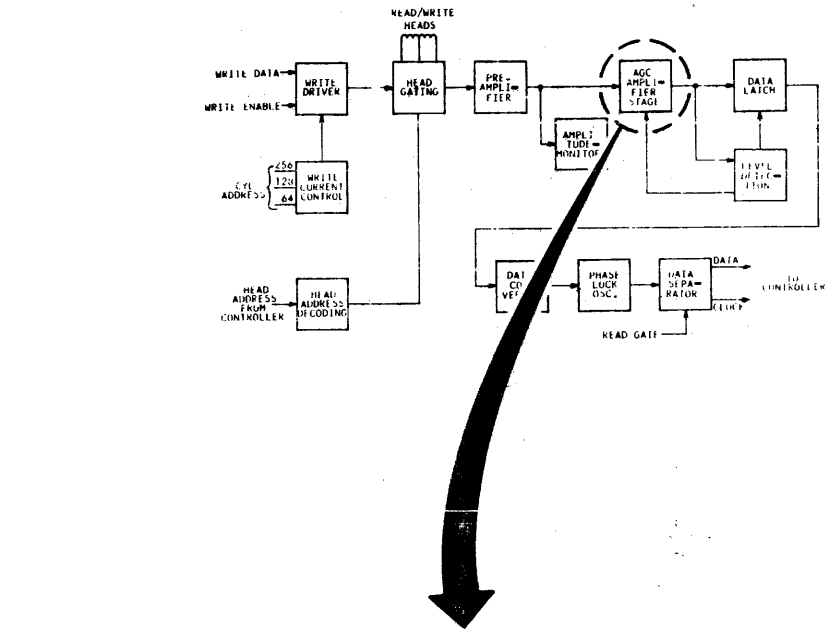


Figure 3-38. Write Chain Timing



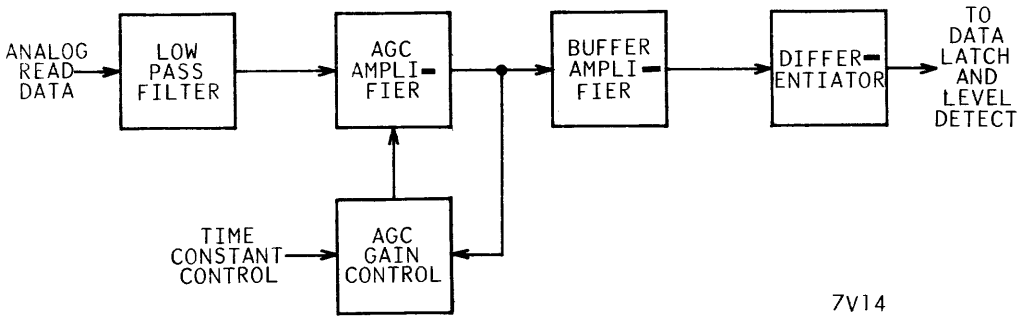


Figure 3-39. AGC Amplifier Stage

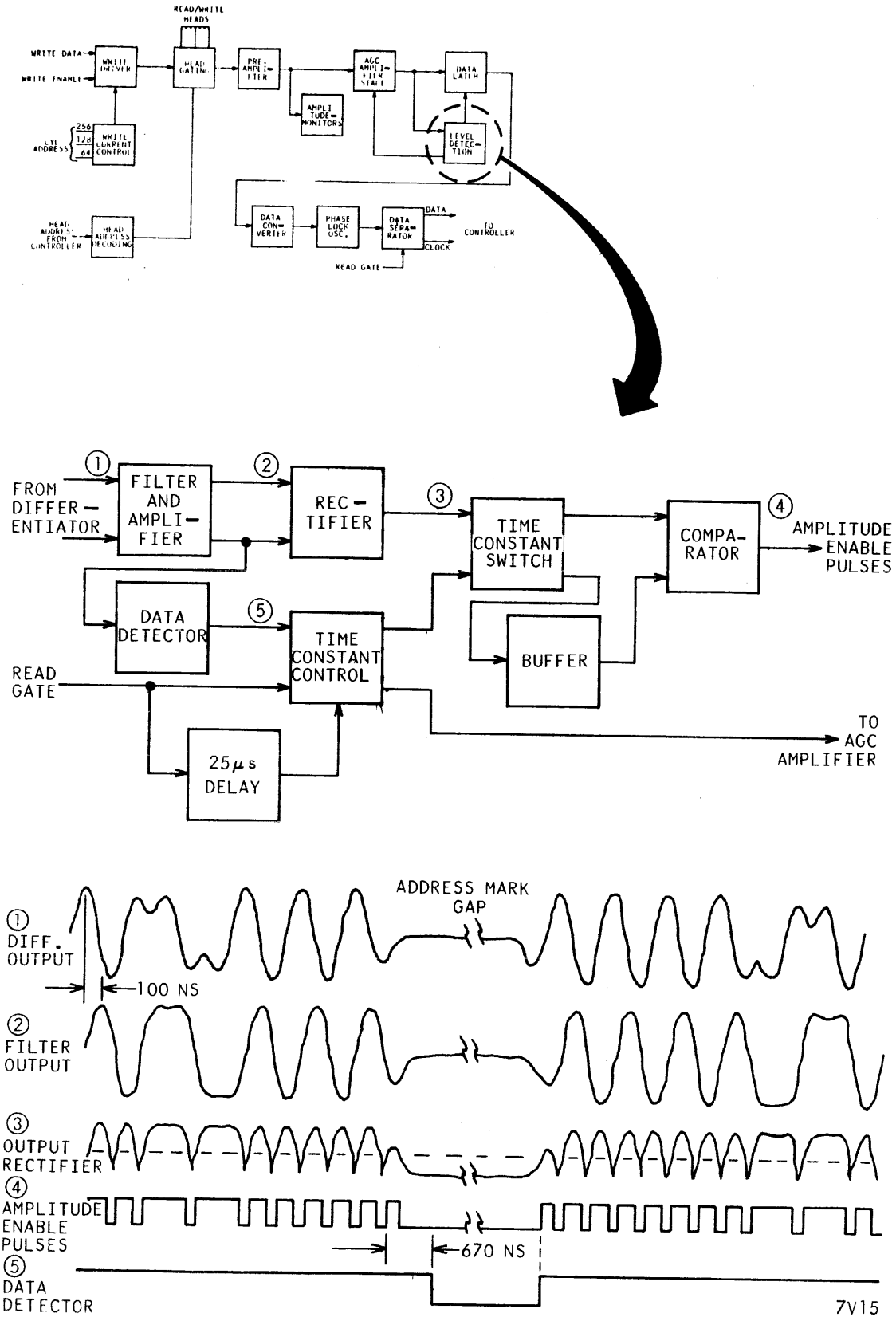


Figure 3-40. Level Detection Circuit

voltage of about -0.46v. Each time the single voltage crosses the reference, the single shot is retriggered. The single shot will not time out as long as data is being read. When a gap is reached, the single shot is retriggered by the last bit preceding the gap, times out for 670 nsec (which is slightly longer than a bit time), then changes state to indicate an absence of data (Figure 3-40). The single shot is retriggered by the first data bit following the gap and by each succeeding bit, indicating that data is again present.

The Time Constant Control circuit switches the time constants of the AGC Amplifier and Level Detection circuits. Switching from a short time constant to a long time constant avoids responding to the loss of amplitude in the address mark gap area. Figure 3-41 shows block and timing diagrams of the Time Constant Control circuit with the address mark gap in three different positions.

The Level Detector circuit is normally in a short time constant of 5 μsec in order to rapidly respond to changes in signal amplitude to maintain adequate margin in the amplitude enable function. The 5 μsec time is long enough so that the level detector does not respond to dropouts caused by disk surface bad spots. During the address mark gap, the level detector is switched to a time constant of 100 μsec. This prevents a shift in the comparator reference level so noise in the gap area does not produce false enable pulses.

The AGC amplifier is allowed 25 μsec to stabilize from the Head Select and Read Gate transients.

Data Latch Circuit

The Data Latch circuit (Figure 3-42) consists of a low pass filter for the low resolution channel and zero-cross detectors and pulse generators for both the high and low resolution channels. The circuit also includes appropriate delays, a latch, and an output pulse former.

The Read Data from the differentiator is applied directly to the zero-cross detector in the high resolution channel and through the low pass filter to the zero-cross detector in the low resolution channel. As mentioned before, the filter lowers the resolution of the Read signal by attenuating the third harmonic of the signal.

The pulse generators (X2500 and X2501) produce pulses for each zero-crossing of the data. By appropriate delays, the low channel pulse sets the latch (I2506) approximately 50 nsec before the high channel pulse resets it (I2505). This produces an output pulse from the latch in which the reset of trailing edge retains the timing of the high resolution channel. A pulse forming circuit produces a 40-nsec data pulse from the trailing edge of the latch output. Note that the propagation time of the various gates must be considered in order to enable AND gate I2513.

The high resolution channel may form extraneous zero crossing pulses caused by the low frequency input dropping through the zero level. These extraneous pulses would follow the legitimate zero-crossing pulse. Therefore, they are ignored by the latch because the latch was reset by the legitimate pulse and can not be reset again unless first set by the low resolution channel. The low channel has no extraneous pulses.

The rejection of spurious pulses in the address mark gap is accomplished by ANDing the high channel pulses with an enable pulse. The Amplitude Enable pulses from the Level Detection circuit are ANDed with the Search Address Mark signal from the controller. During the search mode, the Amplitude Enable pulses are passed through and ANDed with the high channel zero crossover pulses. When a zero crossover pulse corresponds to an enable pulse, it is passed through to reset the latch.

There are noise created zero-crossover pulses in the address mark gap area. However, there are no

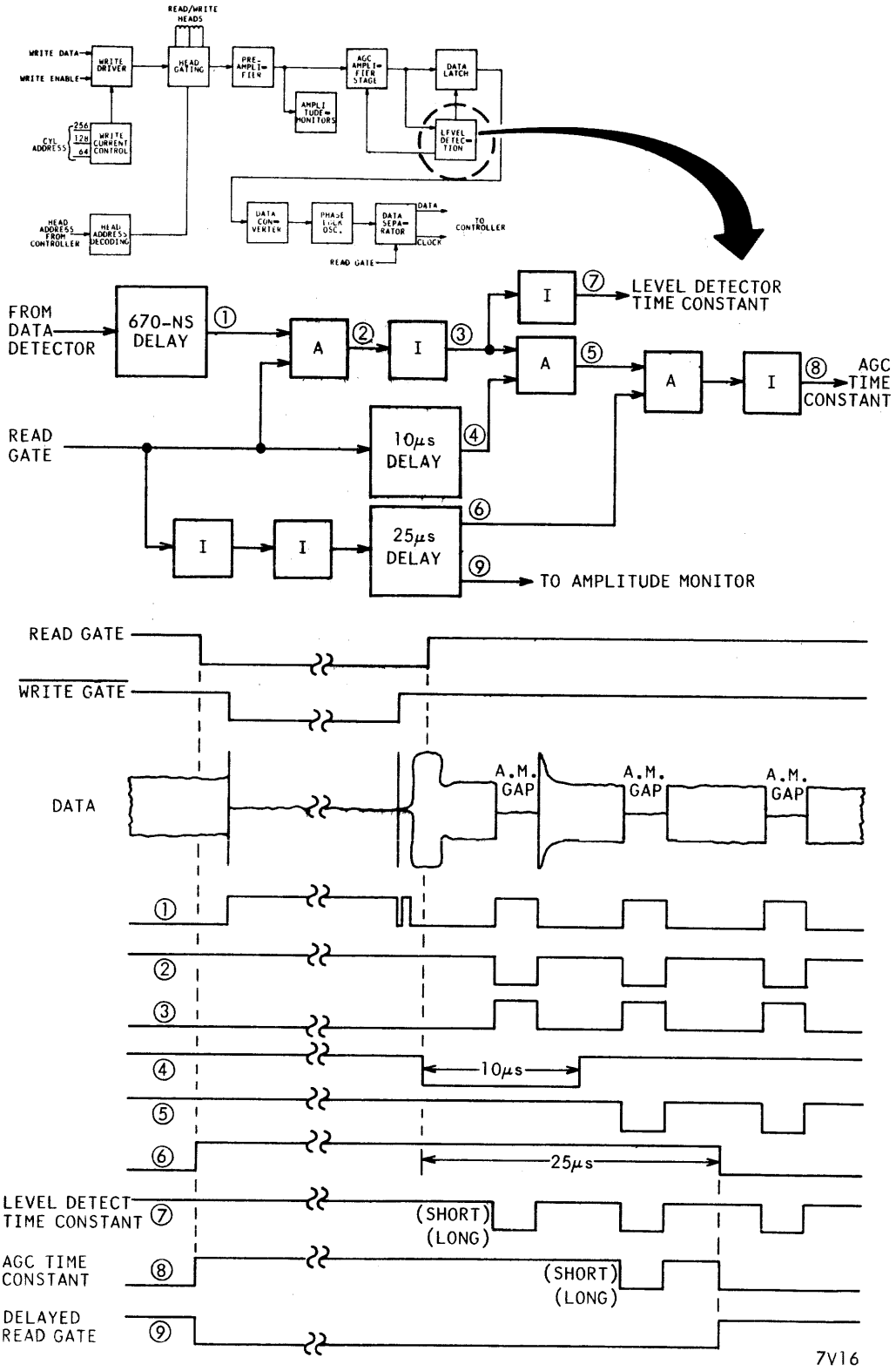


Figure 3-41. Time Constant Control Circuit

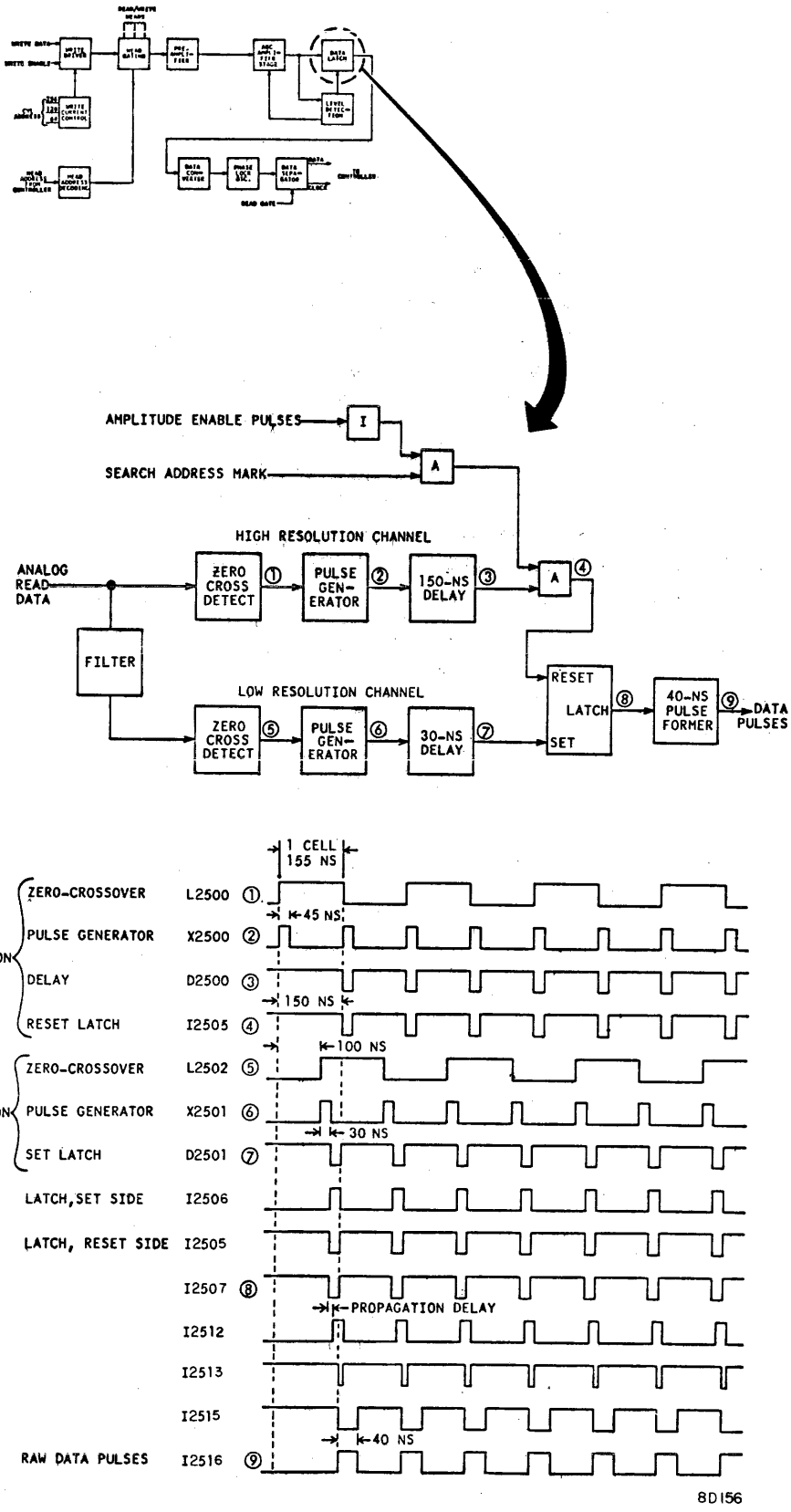


Figure 3-42. Data Latch Circuit

enable pulses, so the reset input to the latch is disabled. Noise pulses in the low resolution channel are present at the set input of the latch, but are ignored because the latch is not reset during the gap period.

The Search Address Mark signal drops at the end of the gap. This applies a constant enable to the high resolution channel and all zero-cross pulses get through to the latch. This terminates the Amplitude Enable function and removes the Level Detector as a possible source of error during the actual reading of data.

Data Converter Circuit

The Data Converter circuit (Figure 3-43) receives the raw data pulses from the Data Latch circuit. Through a series of delay lines and gates, the circuit processes the incoming pulses to form Y Disable pulses (to prevent freewheeling of the phase lock oscillator) and the X and DS pulses. The X and DS pulses are used to sync the phase lock oscillator.

Phase Lock Oscillator

The Phase Lock Oscillator (PLO) provides the synchronized data clock to the Data Separator circuit. The basic phase locked loop is operated at a nominal frequency of 6.4 MHz. The voltage controlled oscillator is slaved to the incoming data and runs at double the loop rate (12.8 MHz). Thus, each of the four phases of the oscillator equals 1/4 cell time and are designated as P1, P2, P3, and P4 time periods.

The Data Sync pulses (X or DS) set the Comparator FF only if they occur in the P1, P2, or P3 time periods (Figure 3-44) when the PLO is running normally (not in a fast start condition). Except in cases of abnormal peak shift, the Comparator FF is set during P1 or P2. A pulse occurring during P3 or P4 is ignored after the FF is set. The DS pulses occur during P1 or P2 periods in a data pattern of all "1's". In a pattern of all "0's", the X pulses occur during P1 or P2. Synchronization shifts between DS and X pulses depending on the data pattern being read. During a data pattern in which neither a DS or X pulse occurs in P1 or P2, the Y Enable pulse is used to set the Comparator FF.

The P4 pulse is used to clear the Comparator FF. This pulse is derived from the difference between the frequency and phase position of the incoming data transitions and that of the phase 4 time period of the voltage controlled oscillator. During normal recovery, this phase is slightly greater than 1/4 cell time. This prevents data pulses, which are in excess of 180° out of phase with a normal data "1" sync pulse, from affecting the output when reading an all "1's" pattern. Under start up conditions, the P4 pulse is reduced to approximately 1/8 cell time to allow incoming data to dominate the Comparator FF.

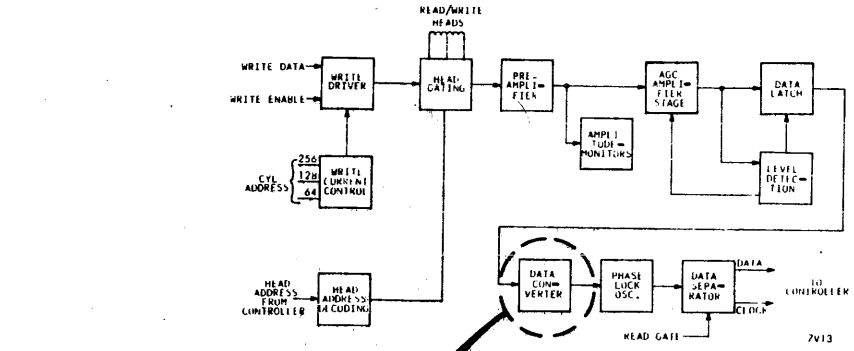
The fast start period increases the loop gain of the PLO so that the correct phase synchronization is accomplished. The control voltage of the oscillator changes rapidly at this time until its dc component has reached the correct value to correspond with the average frequency of the data sync pulses. The squarewave amplitude is also increased to ensure fast phase synchronization.

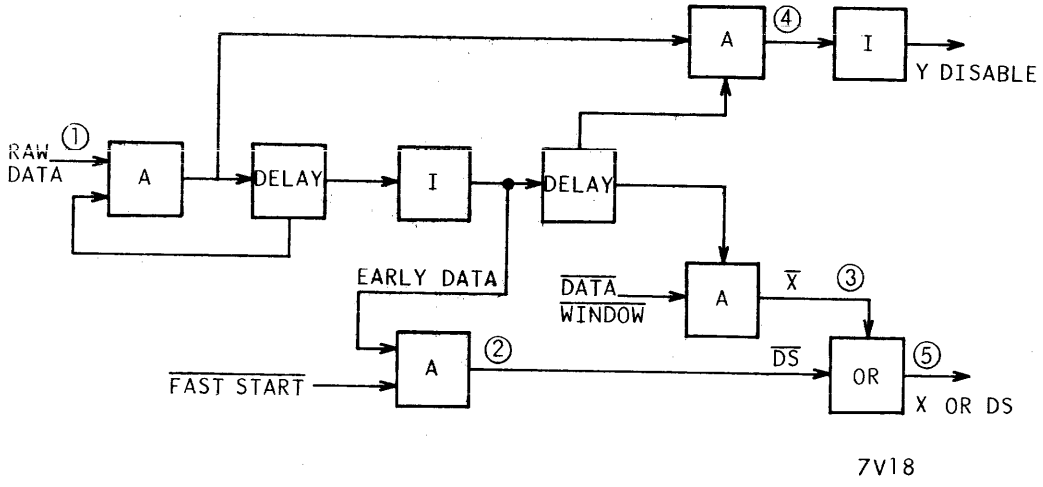
The 5-μsec fast start period is triggered by a Fast Start signal from the controller. A fast start can occur only during a data sync pattern of all "0's". The DS pulses are disabled during fast start. Thus, only X pulses are applied to the Comparator FF.

Data Separator

The Data Separator circuit (Figure 3-45) separates the data "1's" from the clock. The circuit consists of the Data Window FF, Data Detect FF, Data and Clock Register FFs, the Data Strobe circuit, and various delays and gates.

The data window, Shift pulses, and Reset pulses are derived from the $\theta/2$ output of the Phase Lock Oscillator circuit. The data window width is adjustable for maximum data discrimination by means of a tapped delay line. The Data Strobe pulses are used to toggle the Data Detect FF. The nominal strobe is a delayed data pulse. The strobes relative position with respect to the data window is adjusted for





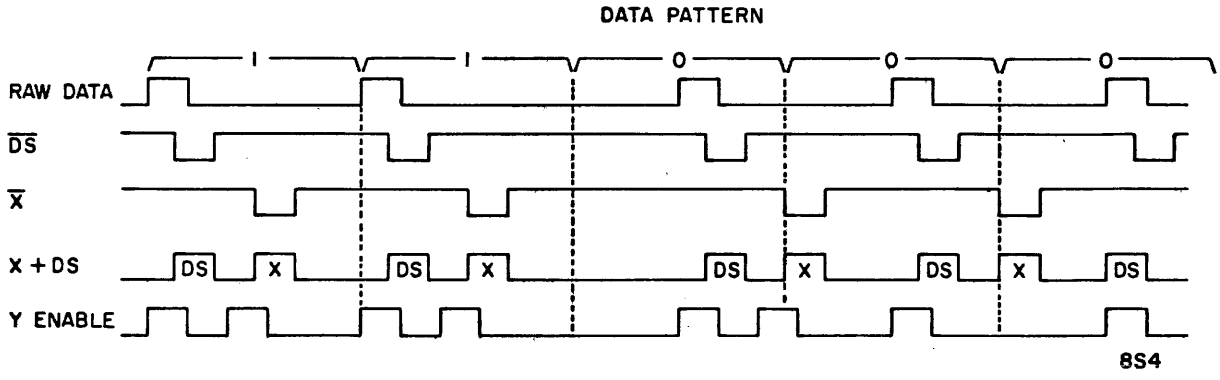


Figure 3-43. Data Converter Circuit.

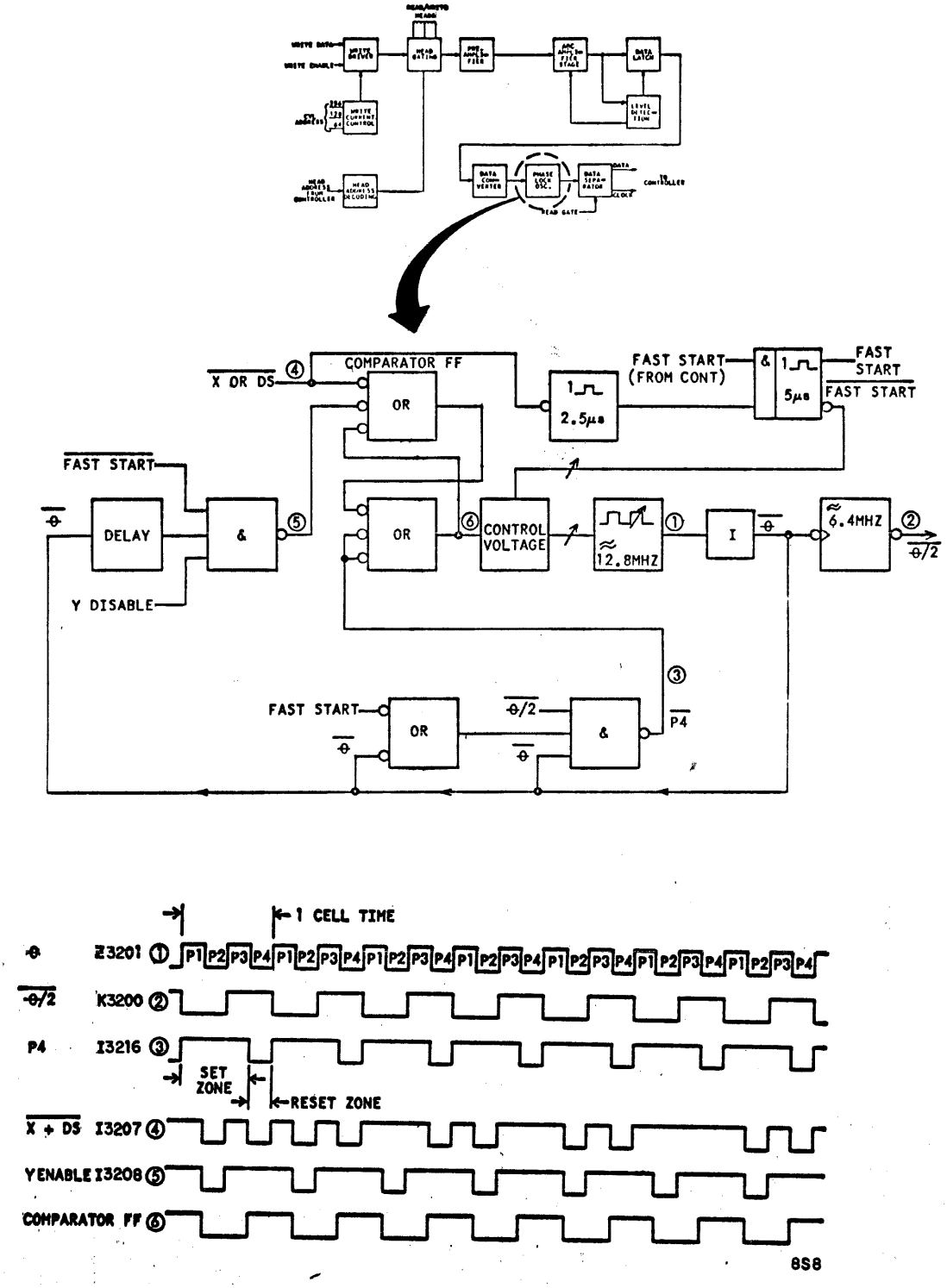


Figure 3-44. Phase Lock Oscillator Circuit

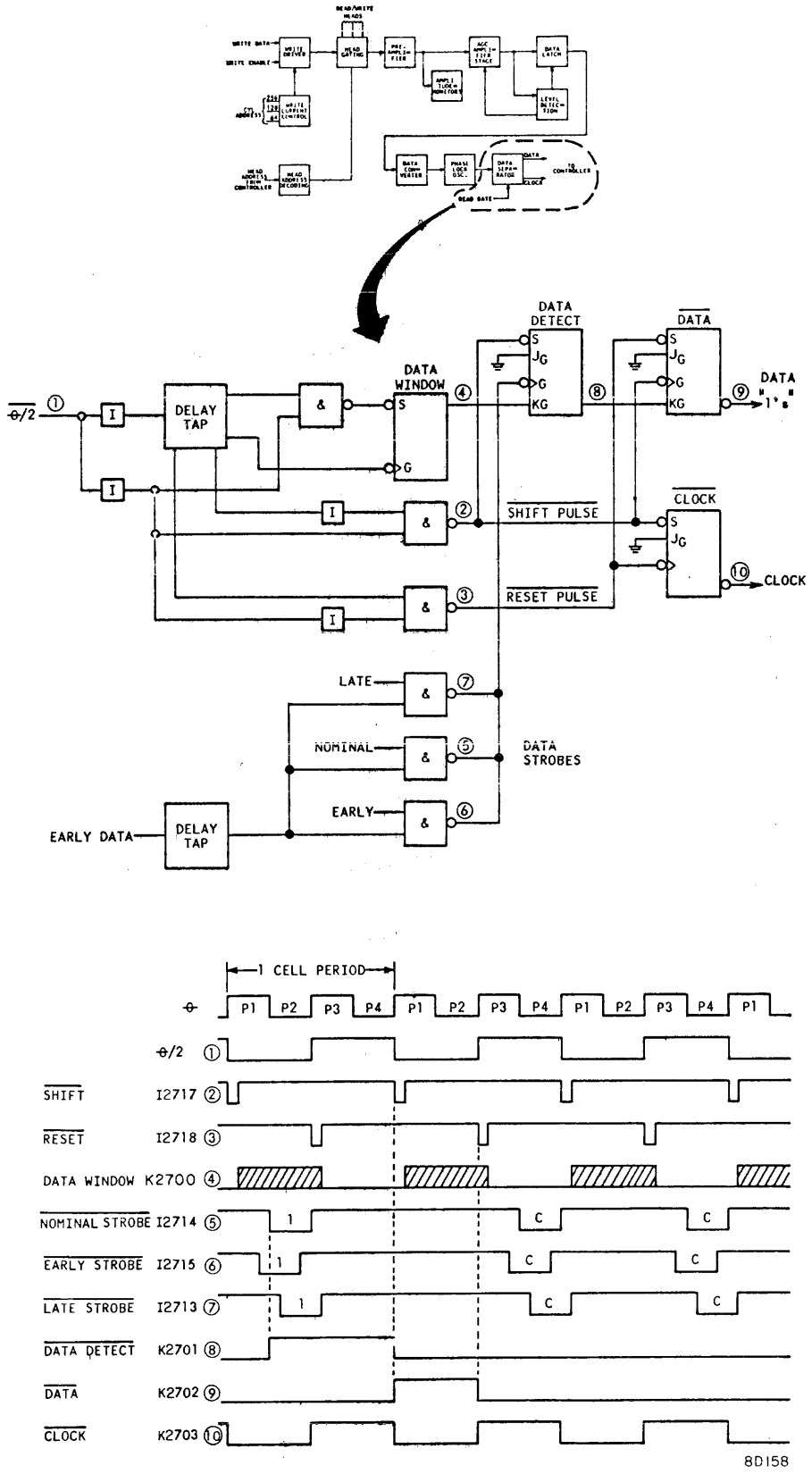


Figure 3-45. Data Separator

maximum data recovery. Early or late strobes may be varied from the nominal strobe time by a command from the controller or the setting of a switch on the logic chassis maintenance panel. This feature allows recovery of data which may be out of position on the disk relative to the average data position.

The Shaft pulses are narrow pulses which occur at the beginning of each cell time. These pulses preset the Data Detect FF and shift the contents of the Data Detect FF into the Data Register FF. The Shift pulses also preset the Clock Register FF.

The Reset pulses also occur once per cell period. They preset the Data Register FF and toggle the Clock Register FF. As shown in Figure 3-45, the Shift and Reset pulses control the timing of the output waveforms of the Data Separator circuit. Note that the data window is delayed beyond the Shift pulse so that the Data Detect FF is always preset in readiness to accept a Data Strobe pulse.

The Data Detect FF is toggled (reset) whenever a Data Strobe occurs during the data window time (Data Window FF set) of a cell period. The next Shift pulse would then transfer the data "1" from the Data Detect FF to the Data Register FF. Note in Figure 3-44 that the data "1" is actually transmitted to the controller one cell time after it is detected.

Read/Write Fault Detection

There are four read/write fault conditions:

(Write OR Read) AND Off Cylinder
Read AND Write
Current
AC Write Fault

The contents of the Fault register can be displayed on the logic chassis maintenance panel. This is accomplished when a Read Fault Status function code is received from the controller or, if the drive is off line, the TAG LINE SELECT switch on the maintenance panel is set to FAULT.

The Fault FF and Fault register latches are cleared by a Clear signal from the controller or the FAULT switch on the logic chassis maintenance panel. The Fault FF output is on a separate I/O line to the controller.

Refer to Figure 3-46 for the following discussions.

(Write OR Read) AND Off Cylinder

This fault is generated if the drive is in an off cylinder condition and it receives a Read or Write Gate from the controller. This condition sets the Fault FF (K2200) and latch I2222/I2223 in the Fault register. The Fault FF, when set, sends a signal to the controller, lights the indicator on the maintenance panel and disables the Write and Access circuits.

Read AND Write

This fault is generated whenever the drive has received both a Read Gate and a Write Gate from the controller. This condition sets the Fault FF and latch I2220/I2221.

Current

A current fault is generated by two conditions: More than one head selected for longer than 7.5 μsec or AC Write Fault.

When more than one head is selected the SCE circuit indicates a Multiple Head Fault (Y2000). The fault is delayed 7.5 μsec by X2101. If the fault exists after the delay, K2100 sets (Multiple Head Select). This sets the Fault FF and latch I2218/I2219 in the fault register.

AC Write Fault

The AC Write fault is generated in both sides of the write driver (L2302) are on or off simultaneously. As long as the write driver is operating properly, threshold detector L2307/L2308 continuously toggles and retriggers single shot X2300. The single shot delay times out if the toggling stops and the AC Write fault is generated. Note that the delay is held in the triggered state if Write Enable is dropped or a Multiple Head fault exists. If the delay is allowed to time out, The Fault FF and latch I2210/I2211 are set.

An AC Write fault is generated when writing the address mark gap. However, the controller sends an Address Mark Read/Write pulse to disable the output of the circuit for 7.5 μsec (X2100), so the Fault FF and Fault register latch are not set.

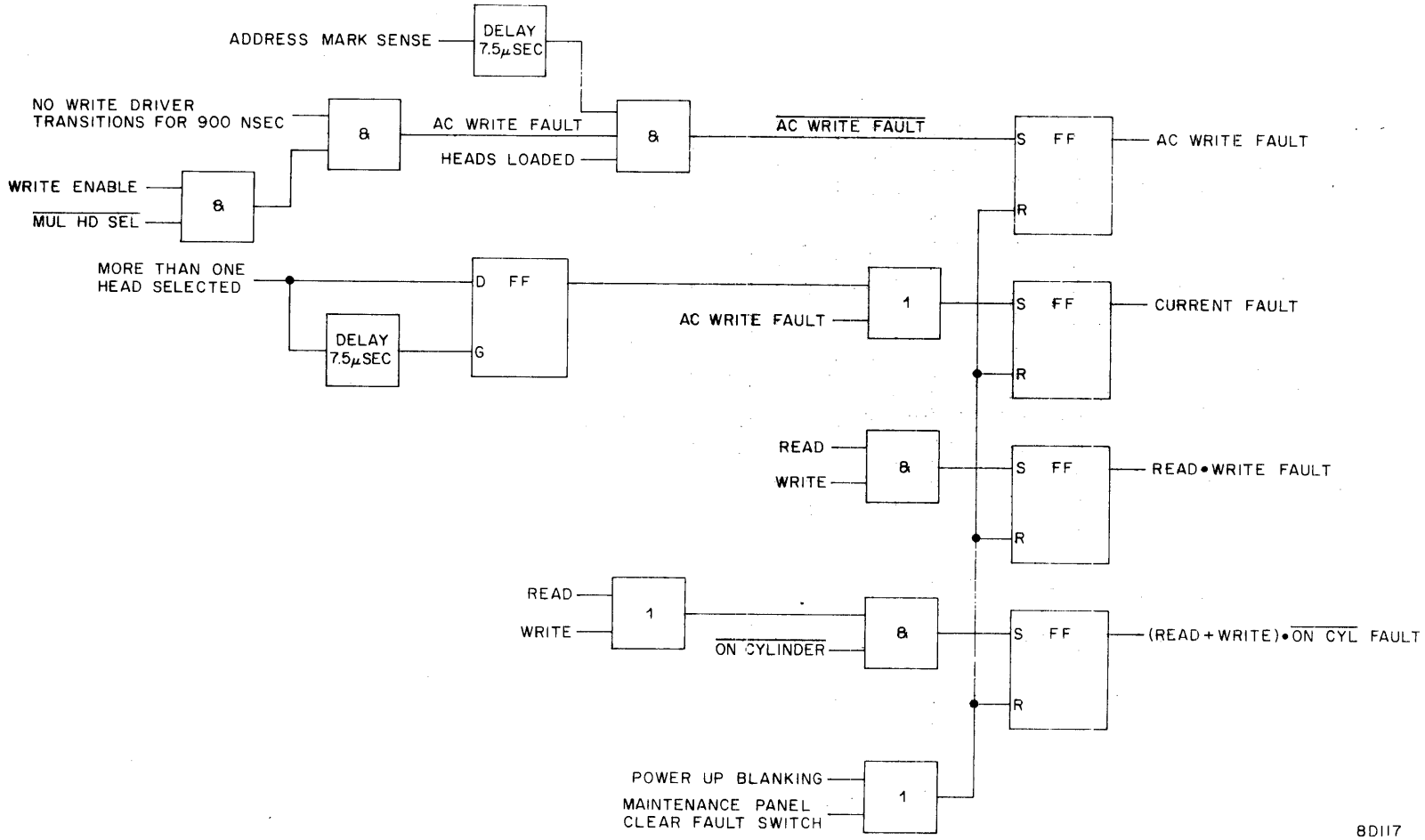
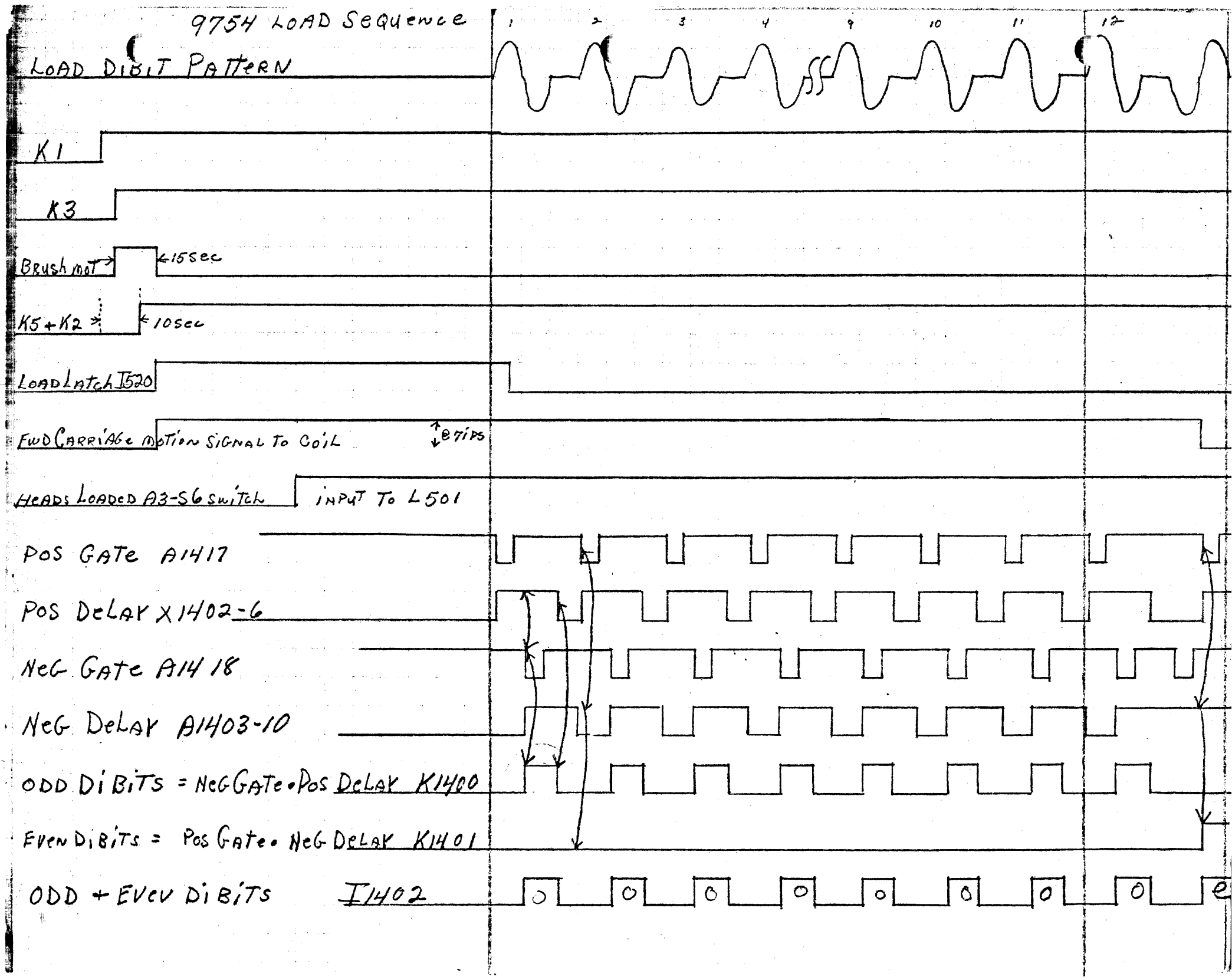
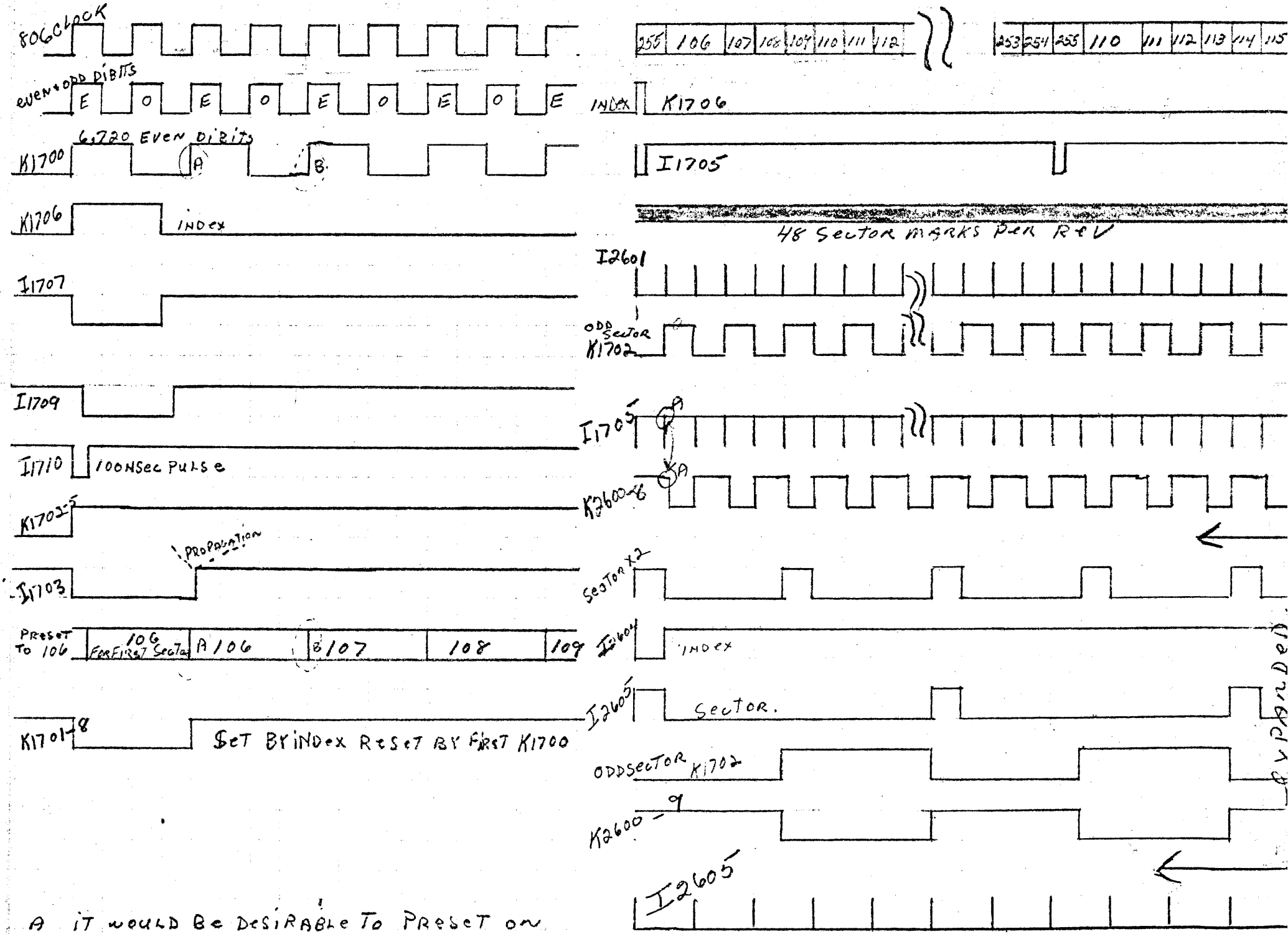
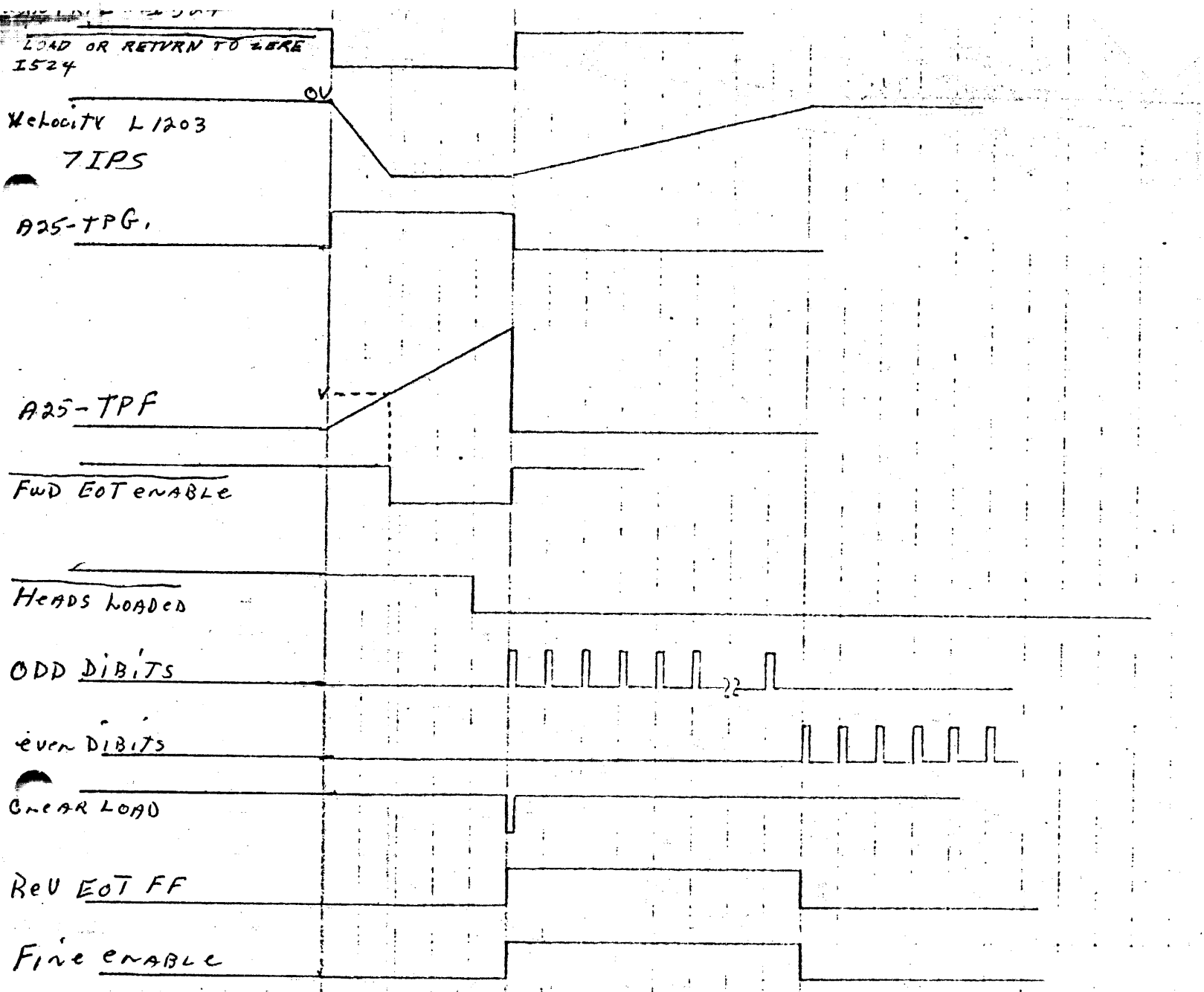


Figure 3-46. Read/Write Fault Detection Circuit


9754 LOAD Sequence
1
2
3
4
9
10
11
12
LOAD DIBIT PATTERN
K1
K3
BRUSH MOT
.15sec
K5 + K2
.10sec
LOAD LATCH I520
FWD CARRIAGE MOTION SIGNAL TO COIL
e7ips
HEADS LOADED A3-S6 SWITCH
INPUT TO L501
POS GATE A1417
POS DELAY X1402-6
NEG GATE A1418
NEG DELAY A1403-10
ODD DIBITS = NEG GATE • POS DELAY K1400
EVEN DIBITS = POS GATE • NEG DELAY K1401
ODD + EVEN DIBITS I1402



A IT WOULD BE DESIRABLE TO PRESET ON (A) WITH A COUNT OF 105 FOR THE FIRST SECTOR (ALL THE OTHER SECTORS WILL BE 110) BUT DUE TO THE PROPAGATION DELAY OF I1703 THRU K1701 WE ARE FORCED



EOT OPERATION (LOAD Sequence)

COMMENT SHEET

PLEASE COMPLETE ITEMS 1 THRU 11

From

(1) NAME
(2) DEPARTMENT OR ATTENTION OF
(3) STREET ADDRESS
(4) CITY AND STATE

Manual Information (From Revision Record)

(5) MANUAL TITLE	
(6) PUBLICATION NO.	(7) REVISION
(8) FCO'S INCORPORATED INTO MANUAL	

Equipment Information (From Equipment Nameplate & FCO Log)

(9) EQUIPMENT NO. AND DESCRIPTION
(10) SERIES CODE
(11) FCO'S INCORPORATED INTO EQUIPMENT

Comments

This form is not intended to be used as an order blank. Your evaluation of this manual will be welcomed by Control Data Corporation. Any errors, suggested additions or deletions, or general comments may be made above. Please include references to figure number, assembly number and design configuration level.

CUT ALONG LINE

KØR 0502 PRINTED IN U.S.A.

NO POSTAGE STAMP NECESSARY IF MAILED IN U. S. A.

FOLD ON DOTTED LINES AND STAPLE

STAPLE

STAPLE

FOLD

FOLD

FIRST CLASS
PERMIT NO. 8241

MINNEAPOLIS, MINN.

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN U.S.A.

POSTAGE WILL BE PAID BY

CONTROL DATA CORPORATION
Technical Publications Department
7801 Computer Avenue
Minneapolis MN 55435

CUT ALONG LINE

FOLD

FOLD

CORPORATE HEADQUARTERS, P.O. BOX 0, MINNEAPOLIS, MINNESOTA 55440
SALES OFFICES AND SERVICE CENTERS IN MAJOR CITIES THROUGHOUT THE WORLD

LITHO IN U.S.A.

CONTROL DATA CORPORATION